#### REMARKS

This is in response to the Office communication mailed on November 22, 2005, and for which a two-month extension is hereby requested. The Office Communication indicated that the previous response failed to comply fully with 37 C.F.R. §41.202(a)(2). The current response provides an expanded version of sections (2) and (3) of the previous response.

Consequently, in response to the various portions of 37 C.F.R. §41.202(a):

### (1) Identification of Patent

Section (1) requires sufficient information to identify the patents with which the interference is sought.

Claims 63-77 are substantial copies claims 1, 3, 4, 6, 13, 15-17, 19, 20, and 29-33, respectively, of U.S. Patent No. 6,014,327 of Banks, granted issue January 11, 2000. Claims 63-72 are also substantial copies of claims 7, 9, 10, 12, 21, 23-25, 27, and 28, respectively, of the Banks '998 nation!

Claims 80-93 are substantial copies claims 1-6 and 13-20, respectively, of U.S. Patent No. 6,344,998 of Banks, granted issue March 12, 2002. Claims 80-93 are also substantial copies of claims 7-12, and 21-28, respectively, of the Banks '998 patent.

Claims 94-98, 100, 102, 104, and 106 are exact copies of claims 1, 3-6, 12, 15, 18, and 21, respectively, of U.S. Patent No. 6,381,172 of Banks, issued April 30, 2002. Claims 99, 101, 103, and 105 are substantial copies of the pairs of claims 7 and 8, 13 and 14, 16 and 17, and 19 and 20, respectively, of U.S. Patent No. 6,381,172.

Claims 107-109, 111, 113-115, 117, 119-121, and 123 are exact copies of claims 1-3, 6, 9-11, 14, 17-19, and 22, respectively, of U.S. Patent No. 6,404,675 of Banks, issued June 11, 2002. Claims 110, 112, 116, 118, 122, and 124 are substantial copies of the pairs of claims 4 and 5, 7 and 8, 12 and 13, 15 and 16, 20 and 21, and 23 and 24, respectively, of U.S. Patent No. 6,404,675.

# (2) Identification of Claims Believed to Interfere, ProposedCount, and Claim Correspondence

Section (2) requires that all claims believed to interfere are identified, that one or more counts is proposed, and that it is shown how the claims correspond to the one or more counts.

Claims 63-72 are substantial copies claims 1, 3, 4, 6, 13, 15-17, 19, and 20, respectively, and of claims 7, 9, 10, 12, 21, 23-25, 27, and 28, respectively, of U.S. Patent No. 6,014,327 and, consequently, so correspond.

Claims 73-77 are substantial copies claims 29-33, respectively, of U.S. Patent No. 6,014,327 and, consequently, so correspond.

Claims 80-93 are substantial copies claims 1-6 and 13-20, respectively, and also of claims 7-12, and 21-28, respectively, of U.S. Patent No. 6,344,998 and, consequently, so correspond.

Claims 94-98, 100, 102, 104, and 106 are exact copies of claims 1, 3-6, 12, 15, 18, and 21, respectively, of U.S. Patent No. 6,381,172 and, consequently, so correspond.

Claims 99, 101, 103, and 105 are substantial copies of the pairs of claims 7 and 8, 13 and 14, 16 and 17, and 19 and 20, respectively, of U.S. Patent No. 6,381,172 and, consequently, so correspond.

Claims 107-109, 111, 113-115, 117, 119-121, and 123 are exact copies of claims 1-3, 6, 9-11, 14, 17-19, and 22, respectively, of U.S. Patent No. 6,404,675 and, consequently, so correspond.

Claims 110, 112, 116, 118, 122, and 124 are substantial copies of the pairs of claims 4 and 5, 7 and 8, 12 and 13, 15 and 16, 20 and 21, and 23 and 24, respectively, of U.S. Patent No. 6,404,675 and, consequently, so correspond.

Consequently, the present application contains claims that are either exact or substantial copies of claims from four patents. As these claims are from four separate patents, the Patent Office has found that these claims correspond to four different inventions; that is, as these claims form four groups, each from a different patent, the implication is that the Office has found the claims within each group to correspond, but that claims from different groups are distinct. Although the validity of this grouping has not been considered in detail, to facilitate the Interference process, the applicant suggests four counts, one corresponding to each group of claims.

Claim 63 of the present application, which is a substantial copy of both claims 1 and 7 of U.S. Patent No. 6,014,327 is suggested as a Count 1:

#### Count 1

For an electrically alterable non-votatite multi-level memory device including a plurality of non-votatile multi-level memory cells, each of the multi-level memory cells including a floating gate FET having a channel with electrically alterable voltage threshold value, the plurality of non-voltalite multi-level memory cells being daposed in a matrix of rows and columns, characles of multi-level memory cells of a first group of the plurality of non-voltalite multi-level memory cells of a first group of the plurality of non-voltalite multi-level memory cells being coupled in parallel between a second bit line and at the reference potential, channels of multi-level memory cells of a second group the plurality of non-voltalite multi-level memory cells being capable of being incided into the folding gate from the channel of each of the plurality of non-voltatile multi-level memory cell, of the channel of each of the plurality of non-voltatile multi-level memory cells of the second group being abstantially flowing in a same duretion, a method of operating the electrically alterable non-volatile multi-level memory device, comprising:

settling a parameter of at least one non-volatile multi-level memory cell of the plurality of non-volatile multi-level memory cells to one state selected from a plurality of states including at least a first state, a second state, a third state and a fourth state in response to information to be stored in the one non-volatile multi-level memory cell.

errifying whether the parameter of the one non-volatile multi-level memory cell has being settled to the one state selected from the plantility of states by comparing the parameter of the one non-volatile multi-level memory cell with a plurality of verifying reference parameters including at least a first verifying reference parameter, a second verifying reference parameter, a second verifying reference parameter and a fourth verifying reference parameter and a fourth verifying reference parameter, as the parameter and the operation for verifying until it is verified by the operation for verifying that the parameter and the operation for verifying that the parameter of the one non-volatile multi-level memory cell has being settled to the one

reading status of the one non-volatile multi-level memory cell by comparing the parameter with a plurality of reading reference parameters including at least a first reading reference parameter, a second reading reference parameter and a third reading reference parameter.

wherein a conductivity value of the one non-volatile multi-level memory cell is decreased in order of the first state, the second state, the third state and the fourth state, wherein the first reading reference parameter is allocated between the first state

and the second state, the second reading reference parameter is allocated between the second state and the third state, and the third reading reference parameter is allocated between the third state and the fourth state.

wherein the first reading reference parameter, the second reading reference parameter and the third reading reference parameter are parameters for a normal read operation in which the information stored in the one non-volatile multi-level memory cell can be read out by output data of a plurality of bits.

wherein the normal read operation is carried out by parallel-comparing the parameter with the plurality of reading reference parameters by using a plurality of sense circuits including at least a first sense circuit, as econd sense circuit and a third sense circuit. first input terminals of the first sense circuit, the second sense circuit and the third sense circuit are commonly supplied with the parameter from the one non-volatile multilevel memory cell, a second input terminal of the first sense circuit is supplied with the first trading reference parameter, a second input terminal of the second sense circuit is

EFS Filing

supplied with the second reading reference parameter and a second input terminal of the third sense circuit is supplied with the third reading reference parameter, and

wherein the first venifying reference parameter is allocated below the first reading reference parameter, the second venifying reference parameter is allocated between the first reading reference parameter and the second reading reference parameter and the second reading reference parameter as allocated between the second reading reference parameter as allocated between the second reading reference parameter and the fourth reading reference parameter and the fourth reading reference parameter is allocated above the third reading reference parameter.

Claims 63-72 are substantial copies claims 1, 3, 4, 6, 13, 15-17, 19, and 20, respectively, and of claims 7, 9, 10, 12, 21, 23-25, 27, and 28, respectively, of U.S. Patent No. 6,014,327 and, consequently, would correspond to Count 1 under the suggested correspondence. Claims 73-77 are substantial copies claims 29-33, respectively, of U.S. Patent No. 6,014,327 and, consequently, would correspond to Count 1 under the suggested correspondence.

Claim 80 of the present application, which is a substantial copy of both claims 1 and 7 of U.S. Patent No. 6.344.998 is suggested as a Count 2:

### Count 2

For an electrically alterable non-volatile multi-level semiconductor memory device including a plurality of non-volatile multi-level memory cells, each of the multi-level memory cells send to the multi-level memory cells including a floating gate FET having a channel with electrically alterable voltage threshold value, the plurality of non-volatile multi-level memory cells being disposed in a matrix of rows and columns, channels of multi-level memory cells of a group of the plurality of non-volatile multi-level memory cells being outpell in parallel between a bit line and a reference potential, electrons being quaphe of being injected into the floating gate from the channel in each of the plurality of non-volatile multi-level memory cells, a method of operating the electrically alterable non-volatile multi-level semiconductor memory device, compression:

setting a parameter of at least one non-volatile multi-level memory cell of the plurality of non-volatile multi-level memory cells to a state selected from a plurality of states including at least a first state, a second state, a third state and a fourth state in response to information to be stored in the one non-volatile multi-level memory cell.

when one of the first thard states is selected, verifying whether the parameter of the one non-volatile multi-level memory cell has been set to the one state, nelading comparing the parameter of the one non-volatile multi-level memory cell with one of a plurality of verifying reference parameters including at least a first verifying reference parameter, a second verifying reference parameter and a third verifying reference parameter, the operation of setting the parameter being conducted until at its verified by the operation of verifying that the parameter being conducted until at its verified by the operation of verified parameters of the one non-volatile multi-level memory cell has been set to the one state.

reading status of the one non-volatile multi-level memory cell, including comparing the parameter of the one non-volatile multi-level memory cell, with a plurality of reading reference parameters including at least a first reading reference parameter, a second reading reference parameter and a third reading reference parameter.

wherein a conductivity value of the one non-volatile multi-level memory cell is increased in order of the first state, the second state, the third state and the fourth state,

Attorney Docket No.: SNDK A06US5

wherein the first reading reference parameter is allocated between the first state and the second state, the second reading reference parameter is allocated between the second state and the third state, and the third reading reference parameter is allocated between the third state and the fourth state.

wherein the first reading reference parameter, the second reading reference parameter and the third reading reference parameter are parameters for a normal read operation in which the information stored in the one non-volatile multi-level memory cell can be read out as output data of a plurality of thits.

wherein the normal read operation includes parallel-comparing the parameter of the on non-volatile multi-level memory cell with the plurality of reading reference parameters using a plurality of sense circuit, an including at least a first sense circuit, as second sense circuit and a third sense circuit, first input terminals of the first sense circuit, the second sense circuit and the third sense circuit are commonly supplied with the parameter of the one non-volatile multi-level memory cell, a second input terminal of the first sense circuit is supplied with the first reading reference parameter, a second input terminal of the second sense circuit is supplied with the second reading reference parameter and a second imput terminal of the third sense circuit is supplied with the third reading reference parameter,

wherein the first ventifying reference parameter is allocated above the first reading reference parameter, the second verifying reference parameter is allocated between the first reading reference parameter and the second reading reference parameter and the third ventifying reference parameter is allocated between the second reading reference parameter and the third reading reference parameter, and

wherein the plumlity of non-volutile multi-level memory cells of the matrix of the rows and the columns are disposed in substantially a retratingle that has first side, a second side, a third side and a fourth side, the first side and the second side miterace with each other substantially perpendicularly, a plumlity of word lines coupled with gate electrodes of floating gate FETs of the multi-level memory cells and the first side of the retangle intersect with each other substantially perpendicularly, a plumlity of bit lines coupled with drains of floating gate FETs of the multi-level memory cells and the second side of the retangle intersect with each other substantially perpendicularly, a row select side of the retangle intersect with each other substantially perpendicularly, a row select lines, and peripheral circuity, including a column select circuit, enter circuits, a data conversion circuit and latkness, distorped at the second side of the retangles.

Claims 80-93 are substantial copies claims 1-5 and 13-20, respectively, and also of claims 7-12, and 21-28, respectively, of U.S. Patent No. 6,344.998 and, consequently, would correspond to Count 2 under the suscessed correspondence.

Claim 94 of the present application, which is an exact copy of claim 1 of U.S. Patent No. 6,381,172, is suggested as a Count 3:

# Count 3

A non-volatile semiconductor memory device comprising:

a plurality of non-volatile memory cells each of which has a threshold voltage representing data of at least two bits, wherein threshold voltages of the plurality of non-volatile memory cells are shiftable among at least three threshold levels which indicate mutually different programming states and which also differ from a threshold level midicating an erase state:

EFS Filing

Attorney Docket No.: SNDK.A06US5 Application No.: 09/759,119

parameter generating circuitry generating a first programming reference parameter, a first read reference parameter, a second programming reference parameter, a second read reference parameter, a third programming reference parameter and a third read reference parameter; and

sensing/program-verifying circuity receiving a parameter which represents threshold voltage of one non-volatile memory cell, the first programming reference parameter, the first read reference parameter, the second programming reference parameter, the second read reference parameter, the third programming reference parameter and the third read reference parameter.

wherein the first read reference parameter is allocated between a level occreporing to the erase state and the first programming reference parameter, the second read reference parameter is allocated between the first programming reference parameter and the count of programming reference parameter, and the third read reference parameter is allocated between the second programming reference parameter and the third reorgamming reference parameter.

wherein the sensing/program-verifying circuitry generates data of at least two bits represented by the one non-volatile memory cell threshold voltage, verifies whether the one non-volatile memory cell threshold voltage is shifted to the threshold tellor indicating a selected one of the programming states, and propraam the one non-volatile memory cell until it is verified that the one non-volatile memory cell threshold levels has been shifted to that threshold level.

wheren the first programming reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a first threshold level of the three threshold levels, the first read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the first threshold level or to the threshold level indicating the crase state, and one of the first programming reference parameter and the first seal reference parameter is shifted from and dependent upon the

wherein the second programming reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a second threshold voltages are shifted to a second threshold voltage are more to detecting whether non-volatile memory cell threshold voltages are more to the second trachold level or to the first threshold level, and one of the second programming threshold level, and one of the second programming of the programming to the pro

wherein the third programming reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a third threshold level of the three threshold levels, the third read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the third threshold level, and one of the third programming reference parameter and the third read reference parameter is shifted from and deependent upon the other.

Claims 94-98, 100, 102, 104, and 106 are exact copies of claims 1, 3-6, 12, 15, 18, and 21, respectively, of U.S. Patent No. 6,381,172 and, consequently, would correspond to Count 3 under the suggested correspondence. Claims 99, 101, 103, and 105 are substantial copies of the pairs of claims 7 and 8, 13 and 14, 16 and 17, and 19 and 20, respectively, of U.S. Patent No. 6,381,172 and, consequently, would correspond to Count 3 under the suggested correspondence.

Attorney Docket No.: SNDK.A06US5

Claim 107 of the present application, which is an exact copy of both claim 1 of U.S.

Patent No. 6,404,675, is suggested as a Count 4:

### Count 4

A non-volatile semiconductor memory device comprising:

a plurality of non-volatile memory cells each of which has a floating gate and a threshold voltage representing data of a least two bits, wherein electrons are capable of the being injected into the floating gate, and wherein threshold voltages of the plurality of mon-volatile memory cells are shiftbale among at least three threshold believeds which indicate muntally different programming states and which also differ from a threshold level indication are area state, and

sensing/program-verifying circuity receiving a parameter which represents the threshold voltage of one non-volatile memory cell, a first programming reference parameter, a first read reference parameter, a second programming reference parameter, a second read reference parameter, a third programming reference parameter and a third read reference parameter.

wherein the first read reference parameter is allocated to represent a level between the drechold level indicating the crass state and a level represented by the first programming reference parameter, the second read reference parameter is allocated between the first programming reference parameter and the second programming reference parameter, and the third read reference parameter is allocated between the reference parameter, and the third read reference parameter is allocated between the parameter.

wherein the sensing/program-verifying circuity generates data of at least two bits represented by the one non-volatile memory cell threshold voltage, verifies whether the one non-volatile memory cell threshold voltage is shifted to the threshold level direction of the control of the memory cell until it is verified that the one non-volatile memory cell threshold voltage has been shifted to that threshold level.

wherein the first programming reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a first threshold level of the three threshold levels, and the first tead reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the first threshold level or to the threshold level indication the erace state.

wherein the second programming reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a second threshold level of the three threshold levels, and the second read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the second threshold level or to the first threshold level.

wherein the third programming reference parameter is used for ventifying whether non-volatile memory cell threshold voltages are shifted to a third threshold level of the three threshold levels, and the third read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the third threshold level or to the second threshold level.

wherein the first read reference parameter, the second read reference parameter and the third read reference parameter are parameters for a normal read operation in which the information stored in the one non-volatile memory cell can be read out as output data of a plurality of bits,

Attorney Docket No.: SNDK.A06US5

wherein the normal read operation includes parallel-comparing the parameter representing the threshold voltage of the one non-voltalle memory cell with the plurality of reading reference parameters using a plurality of sense circuit is necluding all least a first sense circuit, a second sense circuit and a third sense circuit, first input terminals of the first sense circuit, the second sense circuit and the third sense circuit are commonly supplied with the parameter from the one non-voltalle multi-level memory cell, a second input terminal of the first sense circuit is supplied with the first read reference parameter, a second input terminal of the second sense circuit is supplied with the there have developed by the second read reference parameter.

wherein the first read reference parameter is allocated to represent a level between the threshold level indicating the erase state and the first threshold level, the second read reference parameter is allocated to represent a level between the first threshold level, and the second threshold level, and the third read reference parameter is allocated to represent a level between the second threshold level and the third threshold level, and

wherein the level represented by the second read reference parameter is allocated substantially at a midpoint between the first threshold level and the second threshold level, and the level represented by the first read reference parameter is allocated toward the first threshold level from a midpoint between the threshold level indicating the erase state and the first threshold level.

Claims 107-109, 111, 113-115, 117, 119-121, and 123 are exact copies of claims 1-3, 6, 9-11, 14, 17-19, and 22, respectively, of U.S. Patent No. 6,404,675 and, consequently, would correspond to Count 4 under the suggested correspondence. Claims 110, 112, 116, 118, 122, and 124 are substantial copies of the pairs of claims 4 and 5, 7 and 8, 12 and 13, 15 and 16, 20 and 21, and 23 and 24, respectively, of U.S. Patent No. 6,404,675 and, consequently, would correspond to Count 4 under the suggested correspondence.

### (3) Claim Chart for the Counts

Attorney Docket No.: SNDK, A06US5

Section (3) requires a claim chart for the proposed count comparing at least one claim of each party showing why they interfere within the meaning of Sec. 41.203(a).

As the proposed Count 1 is Claim 63 of the present application, they correspond exactly:

Claim 63 of Present Application	Count 1
For an electrically alterable non-	For an electrically alterable non-
volatile multi-level memory device including	volatile multi-level memory device including
a plurality of non-volatile multi-level	a plurality of non-volatile multi-level
memory cells, each of the multi-level	memory cells, each of the multi-level
memory cells including a floating gate FET	memory cells including a floating gate FET

having a channel with electrically alterable voltage threshold value, the plurality of nonvolatile multi-level memory cells being disposed in a matrix of rows and columns, channels of multi-level memory cells of a first group of the plurality of non-volatile multi-level memory cells being coupled in parallel between a first bit line and a reference potential, channels of multi-level memory cells of a second group of the plurality of non-volatile multi-level memory cells being coupled in parallel between a second bit line and the reference potential. electrons being capable of being injected into the floating gate from the channel of each of the plurality of non-volatile multi-level memory cell, electric currents flowing through the channels of the multi-level memory cells of the first group and electric currents flowing through the channels of the multi-level memory cells of the second group being substantially flowing in a same direction, a method of operating the electrically alterable non-volatile multi-level memory device, comprising:

settling a parameter of at least one non-volatile multi-level memory cell of the plurality of non-volatile multi-level memory cells to one state selected from a plurality of states including at least a first state, a second

having a channel with electrically alterable voltage threshold value, the plurality of nonvolatile multi-level memory cells being disposed in a matrix of rows and columns, channels of multi-level memory cells of a first group of the plurality of non-volatile multi-level memory cells being coupled in parallel between a first bit line and a reference potential, channels of multi-level memory cells of a second group of the plurality of non-volatile multi-level memory cells being coupled in parallel between a second bit line and the reference potential, electrons being capable of being injected into the floating gate from the channel of each of the plurality of non-volatile multi-level memory cell, electric currents flowing through the channels of the multi-level memory cells of the first group and electric currents flowing through the channels of the multi-level memory cells of the second group being substantially flowing in a same direction, a method of operating the electrically alterable non-volatile multi-level memory device, comprising:

settling a parameter of at least one non-volatile multi-level memory cell of the plurality of non-volatile multi-level memory cells to one state selected from a plurality of states including at least a first state, a second state, a third state and a fourth state in response to information to be stored in the one non-volatile multi-level memory cell.

verifying whether the parameter of the one non-volatile multi-level memory cell has being settled to the one state selected from the plurality of states by comparing the parameter of the one non-volatile multi-level memory cell with a plurality of verifying reference parameters including at least a first

verifying reference parameter and a fourth verifying reference parameter, and of repeating the operation for settling the parameter and the operation for verifying until it is verified by the operation for verifying that the parameter of the one non-

volatile multi-level memory cell has being

settled to the one state.

verifying reference parameter, a second

verifying reference parameter, a third

reading status of the one non-volatile multi-level memory cell by comparing the parameter with a plurality of reading reference parameters including at least a first reading reference parameter, a second reading reference parameter and a third reading reference parameter, .

wherein a conductivity value of the one non-volatile multi-level memory cell is decreased in order of the first state, the decreased in order of the first state, the

state, a third state and a fourth state in response to information to be stored in the one non-volatile multi-level memory cell.

verifying whether the parameter of the one non-volatile multi-level memory cell has being settled to the one state selected from the plurality of states by comparing the parameter of the one non-volatile multi-level memory cell with a plurality of verifying reference parameters including at least a first verifying reference parameter, a second verifying reference parameter, a third verifying reference parameter and a fourth verifying reference parameter, and of repeating the operation for settling the parameter and the operation for verifying until it is verified by the operation for verifying that the parameter of the one nonvolatile multi-level memory cell has being settled to the one state.

reading status of the one non-volatile multi-level memory cell by comparing the parameter with a plurality of reading reference parameters including at least a first reading reference parameter, a second reading reference parameter and a third reading reference parameter. .

wherein a conductivity value of the one non-volatile multi-level memory cell is

second state, the third state and the fourth second state, the third state and the fourth state.

state wherein the first reading reference

wherein the first reading reference parameter is allocated between the first state and the second state, the second reading reference parameter is allocated between the second state and the third state, and the third reading reference parameter is allocated

between the third state and the fourth state

parameter is allocated between the first state and the second state, the second reading reference parameter is allocated between the second state and the third state, and the third reading reference parameter is allocated between the third state and the fourth state

wherein the first reading reference parameter, the second reading reference parameter and the third reading reference parameter are parameters for a normal read operation in which the information stored in

the one non-volatile multi-level memory cell

can be read out by output data of a plurality

wherein the first reading reference parameter, the second reading reference parameter and the third reading reference parameter are parameters for a normal read operation in which the information stored in the one non-volatile multi-level memory cell can be read out by output data of a plurality of bits.

wherein the normal read operation is carried out by parallel-comparing the parameter with the plurality of reading reference parameters by using a plurality of sense circuits including at least a first sense circuit, a second sense circuit and a third sense circuit, first input terminals of the first sense circuit, the second sense circuit and the third sense circuit are commonly supplied with the parameter from the one non-volatile

multi-level memory cell, a second input

wherein the normal read operation is carried out by parallel-comparing the parameter with the plurality of reading reference parameters by using a plurality of sense circuits including at least a first sense circuit. a second sense circuit and a third sense circuit, first input terminals of the first sense circuit, the second sense circuit and the third sense circuit are commonly supplied with the parameter from the one non-volatile multi-level memory cell, a second input terminal of the first sense circuit is supplied terminal of the first sense circuit is supplied with the first reading reference parameter, a with the first reading reference parameter, a

of hits

second input terminal of the second sense second input terminal of the second sense circuit is supplied with the second reading circuit is supplied with the second reading reference parameter and a second input terminal of the third sense circuit is supplied with the third reading reference parameter, and

reference parameter and a second input terminal of the third sense circuit is supplied with the third reading reference parameter. and

wherein the first verifying reference parameter is allocated below the first reading reference parameter, the second verifying reference parameter is allocated between the first reading reference parameter and the second reading reference parameter, the third verifying reference parameter is allocated between the second reading reference parameter and the third reading reference parameter and the fourth verifying reference parameter is allocated above the third reading reference parameter.

wherein the first verifying reference parameter is allocated below the first reading reference parameter, the second verifying reference parameter is allocated between the first reading reference parameter and the second reading reference parameter, the third verifying reference parameter is allocated between the second reading reference parameter and the third reading reference parameter and the fourth verifying reference parameter is allocated above the third reading reference parameter.

As the proposed Count 1 differs from the claim 1 of U.S. patent number 6.014.327only in the preamble specifying a specific electron injection mechanism (hot electron injection), which does not enter into the claim elements, they also correspond:

Claim 1 of U.S. patent number 6,014,327	Count 1	
For an electrically alterable non-	For an electrically alterable non-	
volatile multi-level memory device including	volatile multi-level memory device including	
a plurality of non-volatile multi-level	a plurality of non-volatile multi-level	
memory cells, each of the multi-level	memory cells, each of the multi-level	
memory cells including a floating gate FET	memory cells including a floating gate FET	
having a channel with electrically alterable	having a channel with electrically alterable	
voltage threshold value, the plurality of non-	voltage threshold value, the plurality of non-	

EFS Filing

volatile multi-level memory cells being volatile multi-level memory cells being disposed in a matrix of rows and columns, disposed in a matrix of rows and columns, channels of multi-level memory cells of a channels of multi-level memory cells of a first group of the plurality of non-volatile first group of the plurality of non-volatile multi-level memory cells being coupled in multi-level memory cells being coupled in parallel between a first bit line and a parallel between a first bit line and a reference potential, channels of multi-level reference potential, channels of multi-level memory cells of a second group of the memory cells of a second group of the plurality of non-volatile multi-level memory plurality of non-volatile multi-level memory cells being coupled in parallel between a cells being coupled in parallel between a second bit line and the reference potential, second bit line and the reference potential, electrons being capable of being injected into electrons being capable of being injected into the floating gate by a phenomenon of hot the floating gate from the channel of each of electron injection from the channel of each of the plurality of non-volatile multi-level the plurality of non-volatile multi-level memory cell, electric currents flowing memory cell, electric currents flowing through the channels of the multi-level through the channels of the multi-level memory cells of the first group and electric memory cells of the first group and electric currents flowing through the channels of the currents flowing through the channels of the multi-level memory cells of the second group multi-level memory cells of the second group being substantially flowing in a same being substantially flowing in a same direction, a method of operating the direction, a method of operating the electrically alterable non-volatile multi-level electrically alterable non-volatile multi-level memory device, comprising: memory device, comprising:

settling a parameter of at least one non-volatile multi-level memory cell of the non-volatile multi-level memory cell of the plurality of non-volatile multi-level memory plurality of non-volatile multi-level memory cells to one state selected from a plurality of cells to one state selected from a plurality of states including at least a first state, a second | states including at least a first state, a second state, a third state and a fourth state in state, a third state and a fourth state in

settling a parameter of at least one

response to information to be stored in the one non-volatile multi-level memory cell.

verifying whether the parameter of the one non-volatile multi-level memory cell has being settled to the one state selected from the plurality of states by comparing the parameter of the one non-volatile multi-level memory cell with a plurality of verifying reference parameters including at least a first verifying reference parameter, a second verifying reference parameter, a third verifying reference parameter and a fourth verifying reference parameter, and of repeating the operation for settling the parameter and the operation for verifying until it is verified by the operation for verifying that the parameter of the one nonvolatile multi-level memory cell has being settled to the one state,

reading status of the one non-volatile parameter with a plurality of reading reference parameters including at least a first reading reference parameter, a second reading reference parameter and a third reading reference parameter, .

wherein a conductivity value of the one non-volatile multi-level memory cell is one non-volatile multi-level memory cell is decreased in order of the first state, the decreased in order of the first state, the second state, the third state and the fourth second state, the third state and the fourth

response to information to be stored in the one non-volatile multi-level memory cell,

verifying whether the parameter of the one non-volatile multi-level memory cell has being settled to the one state selected from the plurality of states by comparing the parameter of the one non-volatile multi-level memory cell with a plurality of verifying reference parameters including at least a first verifying reference parameter, a second verifying reference parameter, a third verifying reference parameter and a fourth verifying reference parameter, and of repeating the operation for settling the parameter and the operation for verifying until it is verified by the operation for verifying that the parameter of the one nonvolatile multi-level memory cell has being settled to the one state.

reading status of the one non-volatile multi-level memory cell by comparing the multi-level memory cell by comparing the parameter with a plurality of reading reference parameters including at least a first reading reference parameter, a second reading reference parameter and a third reading reference narameter. .

wherein a conductivity value of the

of bits

wherein the first reading reference and the second state, the second reading reference parameter is allocated between the second state and the third state, and the third reading reference parameter is allocated between the third state and the fourth state.

wherein the first reading reference parameter, the second reading reference parameter and the third reading reference parameter are parameters for a normal read operation in which the information stored in the one non-volatile multi-level memory cell can be read out by output data of a plurality

wherein the normal read operation is carried out by parallel-comparing the parameter with the plurality of reading reference parameters by using a plurality of sense circuits including at least a first sense circuit, a second sense circuit and a third sense circuit, first input terminals of the first sense circuit, the second sense circuit and the third sense circuit are commonly supplied with the parameter from the one non-volatile multi-level memory cell, a second input terminal of the first sense circuit is supplied with the first reading reference parameter, a second input terminal of the second sense

wherein the first reading reference parameter is allocated between the first state parameter is allocated between the first state and the second state, the second reading reference parameter is allocated between the second state and the third state, and the third reading reference parameter is allocated between the third state and the fourth state

wherein the first reading reference parameter, the second reading reference parameter and the third reading reference parameter are parameters for a normal read operation in which the information stored in the one non-volatile multi-level memory cell can be read out by output data of a plurality of bits.

wherein the normal read operation is carried out by parallel-comparing the parameter with the plurality of reading reference parameters by using a plurality of sense circuits including at least a first sense circuit, a second sense circuit and a third sense circuit, first input terminals of the first sense circuit, the second sense circuit and the third sense circuit are commonly supplied with the parameter from the one non-volatile multi-level memory cell, a second input terminal of the first sense circuit is supplied with the first reading reference parameter, a second input terminal of the second sense

circuit is supplied with the second reading circuit is supplied with the second reading reference parameter and a second input terminal of the third sense circuit is supplied with the third reading reference parameter, and

reference parameter and a second input terminal of the third sense circuit is supplied with the third reading reference parameter. and

wherein the first verifying reference parameter is allocated below the first reading reference parameter, the second verifying reference parameter is allocated between the first reading reference parameter and the second reading reference parameter, the third verifying reference parameter is allocated between the second reading reference parameter and the third reading reference parameter and the fourth verifying reference parameter is allocated above the third reading reference parameter.

wherein the first verifying reference parameter is allocated below the first reading reference parameter, the second verifying reference parameter is allocated between the first reading reference parameter and the second reading reference parameter, the third verifying reference parameter is allocated between the second reading reference parameter and the third reading reference parameter and the fourth verifying reference parameter is allocated above the third reading reference narameter.

As the claims correspond and the present application will prevail on priority, as described in the next section, the claims interfere within the meaning of Sec. 41.203(a).

As the proposed Count 2 is Claim 80 of the present application, they correspond exactly:

Claim 80 of Present Application	Count 2
80. For an electrically alterable non-	For an electrically alterable non-
volatile multi-level semiconductor memory	volatile multi-level semiconductor memory
device including a plurality of non-volatile	device including a plurality of non-volatile
multi-level memory cells, each of the multi-	multi-level memory cells, each of the multi-
level memory cells including a floating gate	level memory cells including a floating gate
FET having a channel with electrically	FET having a channel with electrically
alterable voltage threshold value, the plurality	alterable voltage threshold value, the plurality
of non-volatile multi-level memory cells	of non-volatile multi-level memory cells

being disposed in a matrix of rows and being disposed in a matrix of rows and channel in each of the plurality of nonof operating the electrically alterable non-

columns, channels of multi-level memory columns, channels of multi-level memory cells of a group of the plurality of non- cells of a group of the plurality of nonvolatile multi-level memory cells being volatile multi-level memory cells being coupled in parallel between a bit line and a coupled in parallel between a bit line and a reference potential, electrons being capable of reference potential, electrons being capable of being injected into the floating gate from the being injected into the floating gate from the channel in each of the plurality of nonvolatile multi-level memory cells, a method volatile multi-level memory cells, a method of operating the electrically alterable nonvolatile multi-level semiconductor memory device, comprising:

setting a parameter of at least one non-volatile multi-level memory cell of the

volatile multi-level semiconductor memory

device, comprising:

plurality of non-volatile multi-level memory cells to a state selected from a plurality of states including at least a first state, a second state, a third state and a fourth state in response to information to be stored in the

plurality of non-volatile multi-level memory cells to a state selected from a plurality of states including at least a first state, a second state, a third state and a fourth state in response to information to be stored in the one non-volatile multi-level memory cell,

setting a parameter of at least one

non-volatile multi-level memory cell of the

one non-volatile multi-level memory cell, when one of the first third states is selected, verifying whether the parameter of

the one non-volatile multi-level memory cell has been set to the one state, including comparing the parameter of the one nonvolatile multi-level memory cell with one of a volatile multi-level memory cell with one of a plurality of verifying reference parameters plurality of verifying reference parameters including at least a first verifying reference including at least a first verifying reference parameter, a second verifying reference parameter, a second verifying reference

when one of the first third states is selected, verifying whether the parameter of the one non-volatile multi-level memory cell has been set to the one state, including comparing the parameter of the one nonparameter and a third verifying reference parameter and a third verifying reference parameter, the operation of setting the parameter, the operation of setting the parameter being conducted until it is verified by the operation of verifying that the narameter of the one non-volatile multi-level | narameter of the one non-volatile multi-level memory cell has been set to the one state.

reading status of the one non-volatile multi-level memory cell. comparing the parameter of the one non- comparing the parameter of the one nonvolatile multi-level memory cell, with a volatile multi-level memory cell, with a plurality of reading reference parameters plurality of reading reference parameters including at least a first reading reference including at least a first reading reference parameter, a second reading reference parameter, a second reading reference parameter and a third reading reference parameter and a third reading reference narameter

wherein a conductivity value of the one non-volatile multi-level memory cell is increased in order of the first state, the second state, the third state and the fourth state.

wherein the first reading reference parameter is allocated between the first state and the second state, the second reading reference parameter is allocated between the second state and the third state, and the third reading reference parameter is allocated between the third state and the fourth state.

parameter, the second reading reference parameter and the third reading reference parameter are parameters for a normal read operation in which the information stored in operation in which the information stored in

wherein the first reading reference

parameter being conducted until it is verified by the operation of verifying that the memory cell has been set to the one state.

reading status of the one non-volatile including multi-level memory cell. including parameter.

> wherein a conductivity value of the one non-volatile multi-level memory cell is increased in order of the first state, the second state, the third state and the fourth state.

> wherein the first reading reference parameter is allocated between the first state and the second state, the second reading reference parameter is allocated between the second state and the third state, and the third reading reference parameter is allocated between the third state and the fourth state

> wherein the first reading reference parameter, the second reading reference parameter and the third reading reference parameter are parameters for a normal read

can be read out as output data of a plurality of can be read out as output data of a plurality of hite

the one non-volatile multi-level memory cell the one non-volatile multi-level memory cell bits.

wherein the normal read operation includes parallel-comparing the parameter of the one non-volatile multi-level memory cell with the plurality of reading reference parameters using a plurality of sense circuits including at least a first sense circuit, a second sense circuit and a third sense circuit. first input terminals of the first sense circuit. the second sense circuit and the third sense circuit are commonly supplied with the parameter of the one non-volatile multi-level memory cell, a second input terminal of the first sense circuit is supplied with the first reading reference parameter, a second input terminal of the second sense circuit is supplied with the second reading reference parameter and a second input terminal of the third sense circuit is supplied with the third reading reference parameter,

wherein the normal read operation includes parallel-comparing the parameter of the one non-volatile multi-level memory cell with the plurality of reading reference parameters using a plurality of sense circuits including at least a first sense circuit, a second sense circuit and a third sense circuit first input terminals of the first sense circuit the second sense circuit and the third sense circuit are commonly supplied with the parameter of the one non-volatile multi-level memory cell, a second input terminal of the first sense circuit is supplied with the first reading reference parameter, a second input terminal of the second sense circuit is supplied with the second reading reference parameter and a second input terminal of the third sense circuit is supplied with the third reading reference parameter.

wherein the first verifying reference parameter is allocated above the first reading reference parameter, the second verifying reference parameter is allocated between the first reading reference parameter and the second reading reference parameter and the third verifying reference parameter is allocated between the second reading

wherein the first verifying reference parameter is allocated above the first reading reference parameter, the second verifying reference parameter is allocated between the first reading reference parameter and the second reading reference parameter and the third verifying reference parameter is allocated between the second reading reference parameter and the third reading reference parameter and the third reading reference parameter, and

wherein the plurality of non-volatile substantially perpendicularly, a plurality of bit lines coupled with drains of floating gate FET's of the multi-level memory cells and the second side of the rectangle intersect with each other substantially perpendicularly, a row select circuit is disposed at the first side of the rectangle for coupling with the plurality of word lines, and peripheral circuitry, including a column select circuit, sense circuits, a data conversion circuit and rectangle.

reference parameter, and

wherein the plurality of non-volatile multi-level memory cells of the matrix of the multi-level memory cells of the matrix of the rows and the columns are disposed in rows and the columns are disposed in substantially a rectangle that has a first side, a substantially a rectangle that has a first side, a second side, a third side and a fourth side, the second side, a third side and a fourth side, the first side and the second side intersect with first side and the second side intersect with each other substantially perpendicularly, a each other substantially perpendicularly, a plurality of word lines coupled with gate plurality of word lines coupled with gate electrodes of floating gate FET's of the multi- | electrodes of floating gate FET's of the multilevel memory cells and the first side of the level memory cells and the first side of the rectangle intersect with each other rectangle intersect with each other substantially perpendicularly, a plurality of bit lines coupled with drains of floating gate FET's of the multi-level memory cells and the second side of the rectangle intersect with each other substantially perpendicularly, a row select circuit is disposed at the first side of the rectangle for coupling with the plurality of word lines, and peripheral circuitry, including a column select circuit, sense circuits, a data conversion circuit and latches, is disposed at the second side of the latches, is disposed at the second side of the rectangle.

As the proposed Count 1 differs from the claim 1 of U.S. patent number 6.344.998 only in the preamble specifying a specific electron injection mechanism (hot electron injection), which does not enter into the claim elements, they also correspond:

Claim 1 of U.S. patent number 6,344,998 Count 2 1. For an electrically alterable non-For an electrically alterable nonvolatile multi-level semiconductor memory volatile multi-level semiconductor memory device including a plurality of non-volatile device including a plurality of non-volatile multi-level memory cells, each of the multimulti-level memory cells, each of the multilevel memory cells including a floating gate level memory cells including a floating gate FET having a channel with electrically FET having a channel with electrically alterable voltage threshold value, the plurality alterable voltage threshold value, the plurality of non-volatile multi-level memory cells of non-volatile multi-level memory cells being disposed in a matrix of rows and being disposed in a matrix of rows and columns, channels of multi-level memory columns, channels of multi-level memory cells of a group of the plurality of noncells of a group of the plurality of nonvolatile multi-level memory cells being volatile multi-level memory cells being coupled in parallel between a bit line and a coupled in parallel between a bit line and a reference potential, electrons being capable of reference potential, electrons being capable of being injected into the floating gate by hot being injected into the floating gate from the electron injection from the channel in each of channel in each of the plurality of nonthe plurality of non-volatile multi-level volatile multi-level memory cells, a method memory cells, a method of operating the of operating the electrically alterable nonelectrically alterable non-volatile multi-level volatile multi-level semiconductor memory semiconductor memory device, comprising: device, comprising: setting a parameter of at least one setting a parameter of at least one non-volatile multi-level memory cell of the non-volatile multi-level memory cell of the plurality of non-volatile multi-level memory plurality of non-volatile multi-level memory cells to a state selected from a plurality of cells to a state selected from a plurality of states including at least a first state, a second states including at least a first state, a second state, a third state and a fourth state in state, a third state and a fourth state in response to information to be stored in the response to information to be stored in the one non-volatile multi-level memory cell one non-volatile multi-level memory cell, when one of the first third states is when one of the first third states is selected, verifying whether the parameter of selected, verifying whether the parameter of the one non-volatile multi-level memory cell the one non-volatile multi-level memory cell has been set to the one state, including has been set to the one state, including comparing the parameter of the one nonvolatile multi-level memory cell with one of a volatile multi-level memory cell with one of a plurality of verifying reference parameters including at least a first verifying reference parameter, a second verifying reference parameter and a third verifying reference parameter, the operation of setting the parameter being conducted until it is verified by the operation of verifying that the parameter of the one non-volatile multi-level memory cell has been set to the one state.

memory cell. including comparing the parameter of the one nonvolatile multi-level memory cell, with a plurality of reading reference parameters including at least a first reading reference parameter, a second reading reference parameter and a third reading reference narameter

reading status of the one non-volatile

wherein a conductivity value of the one non-volatile multi-level memory cell is increased in order of the first state, the second state, the third state and the fourth state

wherein the first reading reference parameter is allocated between the first state and the second state, the second reading

comparing the parameter of the one nonplurality of verifying reference parameters including at least a first verifying reference parameter, a second verifying reference parameter and a third verifying reference parameter, the operation of setting the parameter being conducted until it is verified by the operation of verifying that the parameter of the one non-volatile multi-level memory cell has been set to the one state.

reading status of the one non-volatile multi-level memory cell. including comparing the parameter of the one nonvolatile multi-level memory cell, with a plurality of reading reference parameters including at least a first reading reference parameter, a second reading reference parameter and a third reading reference parameter.

wherein a conductivity value of the one non-volatile multi-level memory cell is increased in order of the first state, the second state, the third state and the fourth state.

wherein the first reading reference parameter is allocated between the first state and the second state, the second reading second state and the third state, and the third reading reference parameter is allocated hetween the third state and the fourth state

wherein the first reading reference parameter, the second reading reference parameter and the third reading reference parameter are parameters for a normal read operation in which the information stored in the one non-volatile multi-level memory cell can be read out as output data of a plurality of hits

wherein the normal read operation includes parallel-comparing the parameter of the one non-volatile multi-level memory cell with the plurality of reading reference parameters using a plurality of sense circuits including at least a first sense circuit, a second sense circuit and a third sense circuit first input terminals of the first sense circuit, the second sense circuit and the third sense circuit are commonly supplied with the parameter of the one non-volatile multi-level memory cell, a second input terminal of the first sense circuit is supplied with the first reading reference parameter, a second input terminal of the second sense circuit is supplied with the second reading reference parameter and a second input terminal of the third sense circuit is supplied with the third

reference parameter is allocated between the reference parameter is allocated between the second state and the third state, and the third reading reference parameter is allocated between the third state and the fourth state

wherein the first reading reference parameter, the second reading reference parameter and the third reading reference parameter are parameters for a normal read operation in which the information stored in the one non-volatile multi-level memory cell

can be read out as output data of a plurality of bits. wherein the normal read operation includes parallel-comparing the parameter of the one non-volatile multi-level memory cell with the plurality of reading reference parameters using a plurality of sense circuits including at least a first sense circuit, a second sense circuit and a third sense circuit first input terminals of the first sense circuit. the second sense circuit and the third sense circuit are commonly supplied with the parameter of the one non-volatile multi-level memory cell, a second input terminal of the first sense circuit is supplied with the first reading reference parameter, a second input terminal of the second sense circuit is supplied with the second reading reference parameter and a second input terminal of the third sense circuit is supplied with the third

## reading reference parameter,

wherein the first verifying reference parameter is allocated above the first reading reference parameter, the second verifying reference parameter is allocated between the first reading reference parameter and the second reading reference parameter and the third verifying reference parameter is allocated between the second reading reference parameter, and

wherein the plurality of non-volatile multi-level memory cells of the matrix of the rows and the columns are disposed in substantially a rectangle that has a first side, a second side a third side and a fourth side the first side and the second side intersect with each other substantially perpendicularly, a plurality of word lines coupled with gate electrodes of floating gate FET's of the multilevel memory cells and the first side of the rectangle intersect with each other substantially perpendicularly, a plurality of bit lines coupled with drains of floating gate FET's of the multi-level memory cells and the second side of the rectangle intersect with each other substantially perpendicularly, a row select circuit is disposed at the first side of the rectangle for coupling with the plurality of word lines, and peripheral

# reading reference parameter,

wherein the first verifying reference parameter is allocated above the first reading reference parameter, the second verifying reference parameter is allocated between the first reading reference parameter and the become reading reference parameter and the third verifying reference parameter is allocated between the second reading reference parameter and the third reading reference parameter, and

wherein the plurality of non-volatile multi-level memory cells of the matrix of the rows and the columns are disposed in substantially a rectangle that has a first side, a second side, a third side and a fourth side, the first side and the second side intersect with each other substantially perpendicularly, a plurality of word lines coupled with gate electrodes of floating gate FET's of the multilevel memory cells and the first side of the rectangle intersect with each other substantially perpendicularly, a plurality of bit lines coupled with drains of floating gate FET's of the multi-level memory cells and the second side of the rectangle intersect with each other substantially perpendicularly, a row select circuit is disposed at the first side of the rectangle for coupling with the plurality of word lines, and peripheral circuitry, including a column select circuit, circuitry, including a column select circuit, sense circuits, a data conversion circuit and sense circuits, a data conversion circuit and latches, is disposed at the second side of the latches, is disposed at the second side of the rectangle.

rectangle.

As the claims correspond and the present application will prevail on priority, as described in the next section, the claims interfere within the meaning of Sec. 41.203(a).

As the proposed Count 3 is Claim 94 of the present application, they correct

the present application, they correspond exactly
Count 3
A non-volatile semiconductor
memory device comprising:
a plurality of non-volatile memory
cells each of which has a threshold voltage
representing data of at least two bits, wherein
threshold voltages of the plurality of non-
volatile memory cells are shiftable among at
least three threshold levels which indicate
mutually different programming states and
which also differ from a threshold level
indicating an erase state;
parameter generating circuitry
generating a first programming reference
parameter, a first read reference parameter, a
second programming reference parameter, a
second read reference parameter, a third
programming reference parameter and a third
read reference parameter; and
sensing/program-verifying circuitry
receiving a parameter which represents
threshold voltage of one non-volatile memory

EFS Filing

Attorney Docket No.: SNDK. A06US5

cell, the first programming reference parameter, the first read reference parameter, the second programming reference parameter, the second read reference parameter, the third programming reference parameter and the third read reference parameter.

wherein the first read reference parameter is allocated between a level corresponding to the crass state and the first programming reference parameter, the second read reference parameter is allocated between the first programming reference parameter and the second programming reference parameter, and the third read reference parameter is allocated between the second programming reference parameter and the

third programming reference parameter,

wherein the sensing/programverifying circuitry generates data of at least two bits represented by the one non-volatile memory cell threshold voltage, verifies whether the one non-volatile memory cell threshold voltage is shifted to the threshold level indicating a selected one of the programming states, and programs the one non-volatile memory cell until it is verified that the one non-volatile memory cell threshold voltage has been shifted to that threshold level. wherein the first programming

wherein the first programming

cell, the first programming reference parameter, the first read reference parameter, the second programming reference parameter, the second read reference parameter, the third programming reference parameter and the third read reference parameter.

wherein the first read reference parameter is allocated between a level corresponding to the erase state and the first programming reference parameter, the second read reference parameter is allocated between the first programming reference parameter and the second programming reference parameter, and the third read reference parameter is allocated between the second programming reference parameter and the third programming reference parameter.

wherein the sensing/programverifying circuitry generates data of at least two bits represented by the one non-volatile memory cell threshold voltage, verifies whether the one non-volatile memory cell threshold voltage is shifted to the threshold level indicating a selected one of the programming states, and programs the one non-volatile memory cell until it is verified that the one non-volatile memory cell that the one non-volatile memory cell threshold voltage has been shifted to that threshold level,

programming

first

wherein

reference parameter is used for verifying reference parameter is used for verifying whether non-volatile memory cell threshold whether non-volatile memory cell threshold voltages are shifted to a first threshold level voltages are shifted to a first threshold level of the three threshold levels, the first read of the three threshold levels, the first read reference parameter is used for detecting reference parameter is used for detecting whether non-volatile memory cell threshold whether non-volatile memory cell threshold voltages are near to the first threshold level or voltages are near to the first threshold level or to the threshold level indicating the erase to the threshold level indicating the erase state, and one of the first programming state, and one of the first programming reference parameter and the first read reference parameter is shifted from and dependent upon the other,

wherein the second programming reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a second threshold level of the three threshold levels, the second read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the second threshold level or to the first threshold level, and one of the second programming reference parameter and the second read reference parameter is shifted from and dependent upon the other, and

reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a third threshold level of the three threshold levels, the third read

wherein the third

reference parameter and the first read reference parameter is shifted from and dependent upon the other.

wherein the second programming reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a second threshold level of the three threshold levels, the second read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the second threshold level or to the first threshold level, and one of the second programming reference parameter and the second read reference parameter is shifted from and dependent upon the other. and

wherein the third programming reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a third threshold level of the three threshold levels, the third read

programming

reference parameter is used for detecting reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the third threshold level or to the second threshold level, and one of the third programming reference parameter the third programming reference parameter and the third read reference parameter is and the third read reference parameter is shifted from and dependent upon the other.

whether non-volatile memory cell threshold voltages are near to the third threshold level or to the second threshold level, and one of shifted from and dependent upon the other.

As the proposed Count 3 is an exact copy of claim 1 of U.S. Patent No. 6,381,172 as well, they also correspond:

wen, mey also correspond:		
Claim 1 of U.S. patent number 6,014,327	Count 3	
A non-volatile semiconductor	A non-volatile semiconductor	
memory device comprising:	memory device comprising:	
a plurality of non-volatile memory	a plurality of non-volatile memory	
cells each of which has a threshold voltage	cells each of which has a threshold voltage	
representing data of at least two bits, wherein	representing data of at least two bits, wherein	
threshold voltages of the plurality of non-	threshold voltages of the plurality of non-	
volatile memory cells are shiftable among at	volatile memory cells are shiftable among at	
least three threshold levels which indicate	least three threshold levels which indicate	
mutually different programming states and	mutually different programming states and	
which also differ from a threshold level	which also differ from a threshold level	
indicating an erase state;	indicating an erase state;	
parameter generating circuitry	parameter generating circuitry	
generating a first programming reference	generating a first programming reference	
parameter, a first read reference parameter, a	parameter, a first read reference parameter, a	
second programming reference parameter, a	second programming reference parameter, a	
second read reference parameter, a third	second read reference parameter, a third	
programming reference parameter and a third	programming reference parameter and a third	
read reference parameter; and	read reference parameter, and	
sensing/program-verifying circuitry	sensing/program-verifying circuitry	

EFS Filing

receiving a parameter which represents receiving a parameter which represents threshold voltage of one non-volatile memory cell, the first programming reference parameter, the first read reference parameter, the second programming reference parameter. the second read reference parameter, the third programming reference parameter and the third read reference parameter.

wherein the first read reference parameter is allocated between a level corresponding to the erase state and the first programming reference parameter, the second read reference parameter is allocated between the first programming reference parameter and the second programming reference parameter, and the third read reference parameter is allocated between the second programming reference parameter and the

third programming reference parameter, wherein the sensing/programverifying circuitry generates data of at least two bits represented by the one non-volatile memory cell threshold voltage, verifies whether the one non-volatile memory cell threshold voltage is shifted to the threshold level indicating a selected one of the programming states, and programs the one non-volatile memory cell until it is verified non-volatile memory cell until it is verified that the one non-volatile memory cell that the one non-volatile memory cell threshold voltage has been shifted to that threshold voltage has been shifted to that

threshold voltage of one non-volatile memory cell, the first programming reference parameter, the first read reference parameter. the second programming reference parameter. the second read reference parameter, the third programming reference parameter and the third read reference parameter

wherein the first read reference narameter is allocated between a level corresponding to the crase state and the first programming reference parameter, the second read reference parameter is allocated between the first programming reference parameter and the second programming reference parameter, and the third read reference parameter is allocated between the second programming reference parameter and the third programming reference parameter, wherein the

sensing/programverifying circuitry generates data of at least two bits represented by the one non-volatile memory cell threshold voltage, verifies whether the one non-volatile memory cell threshold voltage is shifted to the threshold level indicating a selected one of the programming states, and programs the one

threshold level,				threshold level,
wherein	the	firet	programming	wherein

programming

dependent upon the other.

reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a first threshold level of the three threshold levels, the first read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the first threshold level or to the threshold level indicating the erase state, and one of the first programming reference parameter and the first read reference parameter is shifted from and

reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a first threshold level of the three threshold levels the first read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the first threshold level or to the threshold level indicating the erase state, and one of the first programming reference parameter and the first read reference parameter is shifted from and dependent upon the other.

wherein the first programming

wherein the second programming reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a second threshold level of the three threshold levels, the second read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the second threshold level or to the first threshold level, and one of the second programming reference parameter and the second read reference parameter is shifted from and dependent upon the other. and

wherein the second programming reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a second threshold level of the three threshold levels, the second read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the second threshold level or to the first threshold level, and one of the second programming reference parameter and the second read reference parameter is shifted from and dependent upon the other. and

wherein the third programming reference parameter is used for verifying whether non-volatile memory cell threshold

wherein the third programming reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a third threshold level voltages are shifted to a third threshold level of the three threshold levels, the third read reference parameter is used for detecting reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the third threshold level or to the second threshold level, and one of or to the second threshold level, and one of the third programming reference parameter and the third read reference parameter is and the third read reference parameter is shifted from and dependent upon the other.

of the three threshold levels, the third read whether non-volatile memory cell threshold voltages are near to the third threshold level the third programming reference parameter shifted from and dependent upon the other.

As the claims correspond and the present application will prevail on priority, as described in the next section, the claims interfere within the meaning of Sec. 41.203(a).

As the proposed Count 4 is Claim 107 of the present application, they correspond exactly:

Claim 107 of Present Application	Count 4
<ol> <li>A non-volatile semiconductor</li> </ol>	A non-volatile semiconductor
memory device comprising:	memory device comprising:
a plurality of non-volatile memory	a plurality of non-volatile memory
cells each of which has a floating gate and a	cells each of which has a floating gate and a
threshold voltage representing data of at least	threshold voltage representing data of at least
two bits, wherein electrons are capable of	two bits, wherein electrons are capable of
being injected into the floating gate, and	being injected into the floating gate, and
wherein threshold voltages of the plurality of	wherein threshold voltages of the plurality of
non-volatile memory cells are shiftable	non-volatile memory cells are shiftable
among at least three threshold levels which	among at least three threshold levels which
indicate mutually different programming	indicate mutually different programming
states and which also differ from a threshold	states and which also differ from a threshold
level indicating an erase state; and	level indicating an erase state; and
sensing/program-verifying circuitry	sensing/program-verifying circuitry
receiving a parameter which represents the	receiving a parameter which represents the

threshold voltage of one non-volatile memory cell, a first programming reference parameter, a first read reference parameter, a second programming reference parameter, a second read reference parameter. programming reference parameter and a third read reference parameter.

wherein the first read reference parameter is allocated to represent a level between the threshold level indicating the erase state and a level represented by the first programming reference parameter, the second read reference parameter is allocated between the first programming reference parameter and the second programming reference parameter, and the third read reference parameter is allocated between the second programming reference parameter and the third programming reference parameter,

wherein the sensing/programverifying circuitry generates data of at least two bits represented by the one non-volatile memory cell threshold voltage, verifies whether the one non-volatile memory cell threshold voltage is shifted to the threshold level indicating a selected one of the programming states, and programs the one non-volatile memory cell until it is verified that the one non-volatile memory cell threshold voltage has been shifted to that threshold voltage has been shifted to that

threshold voltage of one non-volatile memory cell, a first programming reference parameter. a first read reference parameter, a second programming reference parameter, a second read reference parameter programming reference parameter and a third read reference parameter:

wherein the first read reference parameter is allocated to represent a level between the threshold level indicating the erase state and a level represented by the first programming reference parameter, the second read reference parameter is allocated between the first programming reference parameter and the second programming reference parameter, and the third read reference parameter is allocated between the second programming reference parameter and the third programming reference parameter,

wherein the sensing/programverifying circuitry generates data of at least two bits represented by the one non-volatile memory cell threshold voltage, verifies whether the one non-volatile memory cell threshold voltage is shifted to the threshold level indicating a selected one of the programming states, and programs the one non-volatile memory cell until it is verified that the one non-volatile memory cell

threshold level,	threshold level,
wherein the first programming	wherein the first programming
reference parameter is used for verifying	reference parameter is used for verifying
whether non-volatile memory cell threshold	whether non-volatile memory cell threshold
voltages are shifted to a first threshold level	voltages are shifted to a first threshold level
of the three threshold levels, and the first read	of the three threshold levels, and the first read
reference parameter is used for detecting	reference parameter is used for detecting
whether non-volatile memory cell threshold	whether non-volatile memory cell threshold
voltages are near to the first threshold level or	voltages are near to the first threshold level or
to the threshold level indicating the erase	to the threshold level indicating the erase
state,	state,
wherein the second programming	wherein the second programming
reference parameter is used for verifying	reference parameter is used for verifying
whether non-volatile memory cell threshold	whether non-volatile memory cell threshold
voltages are shifted to a second threshold	voltages are shifted to a second threshold
level of the three threshold levels, and the	level of the three threshold levels, and the
second read reference parameter is used for	second read reference parameter is used for
detecting whether non-volatile memory cell	detecting whether non-volatile memory cell
threshold voltages are near to the second	threshold voltages are near to the second
threshold level or to the first threshold level,	threshold level or to the first threshold level,
wherein the third programming	wherein the third programming
reference parameter is used for verifying	reference parameter is used for verifying
whether non-volatile memory cell threshold	whether non-volatile memory cell threshold
voltages are shifted to a third threshold level	voltages are shifted to a third threshold level
of the three threshold levels, and the third	of the three threshold levels, and the third
read reference parameter is used for detecting	read reference parameter is used for detecting

EFS Filing

or to the second threshold level,

Attorney Docket No.: SNDK\_A06US5

wherein the first read reference

wherein the first read reference

or to the second threshold level.

whether non-volatile memory cell threshold voltages are near to the third threshold level voltages are near to the third threshold level

parameter, the second read reference parameter and the third read reference parameter are parameters for a normal read operation in which the information stored in the one non-volatile memory cell can be read out as output data of a plurality of bits,

wherein the normal read operation includes parallel-comparing the parameter representing the threshold voltage of the one non-volatile memory cell with the plurality of reading reference parameters using a plurality of sense circuits including at least a first sense circuit, a second sense circuit and a third sense circuit, first input terminals of the first sense circuit, the second sense circuit and the third sense circuit are commonly supplied with the parameter from the one non-volatile multi-level memory cell, a second input terminal of the first sense circuit is supplied with the first read reference parameter, a second input terminal of the second sense circuit is supplied with the second read reference parameter and a second input terminal of the third sense circuit is supplied with the third read reference parameter.

wherein the first read reference parameter is allocated to represent a level between the threshold level indicating the crase state and the first threshold level, the

parameter, the second read reference parameter and the third read reference parameter are parameters for a normal read operation in which the information stored in the one non-volatile memory cell can be read out as output data of a plurality of bits.

wherein the normal read operation includes parallel-comparing the parameter representing the threshold voltage of the one non-volatile memory cell with the plurality of reading reference parameters using a plurality of sense circuits including at least a first sense circuit, a second sense circuit and a third sense circuit, first input terminals of the first sense circuit, the second sense circuit and the third sense circuit are commonly supplied with the parameter from the one non-volatile multi-level memory cell, a second input terminal of the first sense circuit is supplied with the first read reference parameter, a second input terminal of the second sense circuit is supplied with the second read reference parameter and a second input terminal of the third sense circuit is supplied with the third read reference narameter

wherein the first read reference parameter is allocated to represent a level between the threshold level indicating the erase state and the first threshold level, the second read reference parameter is allocated to represent a level between the first threshold level and the second threshold level, and the third read reference parameter is allocated to represent a level between the second threshold level and the third threshold level, and

second read reference parameter is allocated to represent a level between the first threshold level and the second threshold level, and the third read reference parameter is allocated to represent a level between the second threshold level and the third threshold level and

wherein the level represented by the second read reference parameter is allocated substantially at a midpoint between the first threshold level and the second threshold level, and the level represented by the first read reference parameter is allocated toward the first threshold level from a midpoint the first threshold level from a midpoint between the threshold level indicating the between the threshold level indicating the erase state and the first threshold level.

wherein the level represented by the second read reference parameter is allocated substantially at a midpoint between the first threshold level and the second threshold level, and the level represented by the first read reference parameter is allocated toward crase state and the first threshold level

As the proposed Count 4 is an exact copy of both claim 1 of U.S. Patent No. 6,404,675, they also correspond:

	Claim 1 of U.S. patent number 6,404,675	Count 4
	<ol> <li>A non-volatile semiconductor</li> </ol>	A non-volatile semiconductor
	memory device comprising:	memory device comprising:
	a plurality of non-volatile memory	a plurality of non-volatile memory
	cells each of which has a floating gate and a	cells each of which has a floating gate and a
	threshold voltage representing data of at least	threshold voltage representing data of at least
	two bits, wherein electrons are capable of	two bits, wherein electrons are capable of
	being injected into the floating gate, and	being injected into the floating gate, and
	wherein threshold voltages of the plurality of	wherein threshold voltages of the plurality of
į	non-volatile memory cells are shiftable	non-volatile memory cells are shiftable
i	among at least three threshold levels which	among at least three threshold levels which

indicate mutually different programming states and which also differ from a threshold level indicating an erase state; and

sensing/program-verifying circuitry receiving a parameter which represents the threshold voltage of one non-volatile memory cell, a first programming reference parameter, a second programming reference parameter, a second read reference parameter, a third programming reference parameter at third programming reference parameter and a third read reference parameter and a third read reference parameter.

wherein the first read reference parameter is allocated to represent a level between the threshold level indicating the crase state and a level represented by the first programming reference parameter, the second read reference parameter is allocated between the first programming reference parameter and the second programming reference parameter, and the third read reference parameter is allocated between the second programming reference parameter and the third programming reference parameter.

verifying circuitry generates data of at least two bits represented by the one non-volatile memory cell threshold voltage, verifies whether the one non-volatile memory cell threshold voltage is shifted to the threshold

sensing/program-

indicate mutually different programming states and which also differ from a threshold level indicating an erase state; and

sensing/program-verifying circuitry receiving a parameter which represents the threshold voltage of one non-volatile memory coll, a first programming reference parameter, a second programming reference parameter, a second programming reference parameter, a third programming reference parameter, a third programming reference parameter and a third read reference parameter and a third read reference parameter.

wherein the first read reference parameter is allocated to represent a level between the threshold level indicating the crass state and a level represented by the first programming reference parameter, the second read reference parameter is allocated between the first programming reference parameter and the second programming reference parameter, and the third read reference parameter is allocated between the second programming reference parameter and the third programming reference parameter.

wherein the sensing/programverifying circuitry generates data of at least two bits represented by the one non-volatile memory cell threshold voltage, verifies whether the one non-volatile memory cell threshold voltage is shifted to the threshold

wherein the

level indicating a selected one of the programming states, and programs the one non-volatile memory cell until it is verified that the one non-volatile memory cell threshold voltage has been shifted to that threshold level,

wherein the first programming ference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a first threshold level of the three threshold levels, and the first read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the first threshold level or to the threshold level indicating the erase state,

reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a second threshold level of the three threshold levels, and the second read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the second threshold level or to the first threshold level, wherein the third programming.

wherein the second programming

reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a third threshold level of the three threshold levels, and the third

level indicating a selected one of the programming states, and programs the one non-volatile memory cell until it is verified that the one non-volatile memory cell threshold voltage has been shifted to that threshold level,

wherein the first programming ference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a first threshold level of the three threshold levels, and the first read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the first threshold level or to the threshold level indicating the erase state,

wherein the second programming reference parameter is used for venifying whether non-volatile memory cell threshold voltages are shifted to a second threshold level of the three threshold levels, and the second read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the second threshold level or to the first threshold level,

wherein the third programming reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a third threshold level of the three threshold levels, and the third read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the third threshold level or to the second threshold level

wherein the first read reference parameter, the accornd read reference parameter and the third read reference parameter are parameters for a normal read operation in which the information stored in the one non-volatile memory cell can be read out as output data of a plurality of bits,

wherein the normal read operation includes parallel-comparing the parameter representing the threshold voltage of the one non-volatile memory cell with the plurality of reading reference parameters using a plurality of sense circuits including at least a first sense circuit, a second sense circuit and a third sense circuit, first input terminals of the first sense circuit, the second sense circuit and the third sense circuit are commonly supplied with the parameter from the one non-volatile multi-level memory cell, a second input terminal of the first sense circuit is supplied with the first read reference parameter, a second input terminal of the second sense circuit is supplied with the second read reference parameter and a second input terminal of the third sense circuit is supplied with the third read reference

read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the third threshold level or to the second threshold level,

wherein the first read reference parameter, the second read reference parameter and the third read reference parameter are parameters for a normal read operation in which the information stored in the one non-volatile memory cell can be read out as output data of a plurality of bits,

out as output data of a plurality of hits. wherein the normal read operation includes parallel-comparing the parameter representing the threshold voltage of the one non-volatile memory cell with the plurality of reading reference parameters using a plurality of sense circuits including at least a first sense circuit, a second sense circuit and a third sense circuit, first input terminals of the first sense circuit, the second sense circuit and the third sense circuit are commonly supplied with the parameter from the one non-volatile multi-level memory cell, a second input terminal of the first sense circuit is supplied with the first read reference parameter, a second input terminal of the second sense circuit is sunnlied with the second read reference narameter and a second input terminal of the third sense circuit is supplied with the third read reference

parameter,
wherein the first read reference
parameter is allocated to represent a level
between the threshold level indicating the
erase state and the first threshold level, the
second read reference parameter is allocated
to represent a level between the first
threshold level and the second threshold
level, and the third read reference parameter
is allocated to represent a level between the
second threshold level and the third threshold
level, and
wherein the level represented by the
second read reference parameter is allocated
substantially at a midpoint between the first
threshold level and the second threshold
level, and the level represented by the first
read reference parameter is allocated toward
the first threshold level from a midpoint
between the threshold level indicating the
crasc state and the first threshold level.

As the claims correspond and the present application will prevail on priority, as described in the next section, the claims interfere within the meaning of Sec. 41.203(a).

### (4) How Applicant Will prevail on Priority

Section (4) requires an explanation of why the applicant will prevail on priority.

As specified in the "Cross-Reference to Related Application" section added to the beginning of the present application by Preliminary Amendment filed concurrently with the present application, and as is also shown on the filing receipt, the present application is a continuation of U.S. patent application serial number 09/188,417, filed on November 9, 1998, now U.S. patent number 6,304,485, which is which is a continuation of U.S. patent application EFS Filino

Attorney Docket No.: SNDK.A06US5

serial number 08/71,708, filed on December 20, 1996, now U.S. patent number 5,991,517, which is in turn a continuation of U.S. patent application serial number 08/174,768, filed December 29, 1993, now U.S. patent number 5,602,987, which is in turn a continuation of U.S. patent application serial number 07/963,838, filed on October 20, 1992, now U.S. patent number 5,297,148, which is a division of U.S. patent application serial number 07/337,566, filed on April 13, 1989, now abandoned. Consequently, the present application is entitled to an effective filing date of April 13, 1989.

U.S. patent 6,014,327 of Banks has a filing date of May 14, 1999, and claiming priority from a number of U.S. patent applications (in one case through a continuation in-part), the earliest of which has a filing date of February 8, 1991. Thus, this earliest priority date is well over a year after the priority date to which the present amplication is entitled.

Similarly, U.S. patent 6,344,998 of Banks has a filing date of February 8, 2001, and claiming priority from a number of U.S. patent applications, the earliest of which has a filing date of February 8, 1991. Thus, this earliest priority date is well over a year after the priority date to which the present application is entitled.

Similarly, U.S. patent 6,381,172 of Banks has a filing date of May 14, 1999, and claiming priority from a number of U.S. patent applications (in one case through a continuation in-part), the earliest of which has a filing date of February 27, 1995. Thus, this earliest priority date is several years after the priority date to which the present application is intitled

Similarly, U.S. patent 6,404,675 of Banks has a filing date of June 11, 2002, and claiming priority from a number of U.S. patent applications, the earliest of which has a filing date of February 8, 1991. Thus, this earliest priority date is well over a year after the priority date to which the present application is entitled

### (5,6) Claim Charts

The following claim charts are as previously submitted. They show the corresponding written description for each claim in the specification of the present application. They also show where the disclosure provides a constructive reduction to practice within the scope of the interfering subject matter.

Support for Claims

EFS Filing

Attorney Docket No.: SNDK.A06US5

Pending Claims

Present Application

63. For an electrically alterable nonvolatile multi-level memory device including are multi-level na
a plurality of non-volatile multi-level FET memory cells.
memory cells, each of the multi-level
memory cells including a floating gate FET
having a channel with electrically alterable

All of the exemplary embodiments are multi-level non-volatile, floating gate FET memory cells.

voltage threshold value, the plurality of nonvolatile multi-level memory cells being disposed in a matrix of rows and columns, channels of multi-level memory cells of a first group of the plurality of non-volatile

Exemplary array structures with the described matrix structure are shown in Figures 15a and 15b of '344 and Figures 12 and 22 of the present application.

multi-level memory cells being coupled in parallel between a first bit line and a reference potential, channels of multi-level memory cells of a second group of the plurality of non-volatile multi-level memory

> The injection mechanism is described briefly at column 1, lines 42-47, of '344 and in more detail for various cell embodiments beginning at column 5, line 33. See also page 11, lines 18-19 of Preliminary Amendment.

second bit line and the reference potential, electrons being capable of being injected into be the floating gate from the channel of each of it the plurality of non-volatile multi-level be memory cell, electric currents flowing I

through the channels of the multi-level

cells being coupled in parallel between a

memory cells of the first group and electric currents flowing through the channels of the multi-level memory cells of the second group being substantially flowing in a same direction, a method of operating the electrically alterable non-volatile multi-level memory device, comprisine:

EFS Filing Attorney Docket No.: SNDK.A06USS non-volatile multi-level memory cell of the column 25, lines 16-20, of '344, and step 6 of plurality of non-volatile multi-level memory | Figure 23 of the present application. The cells to one state selected from a plurality of states are shown in terms of threshold voltage states including at least a first state, a second in Figure 15A of the present application. See state, a third state and a fourth state in also Figure 11c of '344 for the currentresponse to information to be stored in the one non-volatile multi-level memory cell.

settling a parameter of at least one

verifying whether the parameter of the one non-volatile multi-level memory cell has Also, steps 4 and 5 of Figure 23 of the being settled to the one state selected from present application. the plurality of states by comparing the parameter of the one non-volatile multi-level memory cell with a plurality of verifying reference parameters including at least a first for the verifying reference parameters (the verifying reference parameter, a second Invest) and the corresponding circuitry. verifying reference parameter, a third verifying reference parameter and a fourth verifying reference parameter, and of repeating the operation for settling the parameter and the operation for verifying until it is verified by the operation for Also, the "repeating the operation..." verifying that the parameter of the one non- corresponds to the loop of steps 4, 5, and 6 of

reading status of the one non-volatile multi-level memory cell by comparing the '344 and the corresponding description parameter with a plurality of reading beginning at line 34 of column 26 for the reference parameters including at least a first reading reference parameters (the Inss) and

"Settling" is the program pulse, voltage relation of the states, which is the same as Figure 15B of the present application.

See column 26, lines 18-35, of '344,

See also Figures 11c and 11e of '344

Column 25, lines 16-20, of '338, volatile multi-level memory cell has being Figure 23 of the present application.

See again Figures 11c and 11e of

settled to the one state.

reading reference parameter, a second reading	the corresponding circuitry. See also page
reference parameter and a third reading	12, starting at line 6, of the Preliminary
reference parameter, .	Amendment.
wherein a conductivity value of the	Figures 11c of '338 and 15A and 15B
one non-volatile multi-level memory cell is	of the present application.
decreased in order of the first state, the	
second state, the third state and the fourth	
state,	
wherein the first reading reference	Figures 11c and 11e and column 26,
parameter is allocated between the first state	lines 36-65, of '344.
and the second state, the second reading	
reference parameter is allocated between the	
second state and the third state, and the third	
reading reference parameter is allocated	
between the third state and the fourth state,	
wherein the first reading reference	See again Figures 11c and 11e of
parameter, the second reading reference	'344 and the corresponding description
parameter and the third reading reference	beginning at column 26, lines 36-65, of '344.
parameter are parameters for a normal read	
operation in which the information stored in	
the one non-volatile multi-level memory cell	
can be read out by output data of a plurality	
of bits,	
wherein the normal read operation is	Figure 11e of '344 and column 26,
carried out by parallel-comparing the	lines 4-17 and 39-42. The sense circuits
parameter with the plurality of reading	(SENSE AMPs) are commonly connected in
reference parameters by using a plurality of	parallel to the BIT LINE and receive the
sense circuits including at least a first sense	respective reference currents.
circuit, a second sense circuit and a third	
sense circuit, first input terminals of the first	

sense circuit, the second sense circuit and the third sense circuit are commonly supplied with the parameter from the one non-volatile multi-level memory cell, a second input terminal of the first sense circuit is supplied with the first reading reference parameter, a second input terminal of the second sense circuit is supplied with the second reading reference parameter and a second input terminal of the third sense circuit is sunnlied with the third reading reference parameter. and

The relation of the verifying reference

wherein the first verifying reference parameter is allocated below the first reading parameters and the reading reference reference parameter, the second verifying parameters is described in '344, column 26, reference parameter is allocated between the lines 51-65. first reading reference parameter and the second reading reference parameter, the third verifying reference parameter is allocated between the second reading reference parameter and the third reading reference parameter and the fourth verifying reference parameter is allocated above the third reading reference parameter.

The method of operating the As noted above, the "settling the electrically alterable non-volatile multi-level parameter" is a program operation. Electrons memory according to claim 63, wherein the being injected into the floating gate is operation for settling the parameter includes a standard Flash memory operation; see, for program operation in which electrons are example, column 1, lines 20-28, of '344,

injected into a floating gate of the one nonvolatile multi-level memory cell.

Claims 65 and 66 differ from claims 63 and 64, respectively, in the replacement of "a parameter" with "an electrical value" and in the replacement of "settling a parameter" with "controlling an electrical value". As noted above in the support for claim 63, the "parameter" can be taken as the threshold voltage and the "settling" or "controlling" is the application of a programming pulse. Consequently, the support for claims 65 and 66 is respectively the same as that for 63 and 64 and will not be repeated to save space.

Claims 67 and 68 are device claims that directly correspond, respectively, to method claims 63 and 64 on an element by element basis. Consequently, the support for claims 67 and 68 is again respectively the same as that for 63 and 64 and will also not be repeated to save space.

The electrically alterable nonvolatile multi-level memory according to shown in Figures 15a and 15b of '344 and claim 68, further comprising, a plurality of bit | Figures 12 and 22 of the present application. lines, including said first and said second bit line, each of which transfers information indicating data stored in a memory cell, wherein drain regions of said multi-level memory cells of said first group in said matrix are coupled to said first bit line of said plurality of bit lines, drain regions of said multi-level memory cells of said second group adjoining to said first group in said matrix are coupled to said second bit line adjoining to said first bit line in said plurality

The described matrix structure is

of bit lines and drain regions of multi-level
memory cells of a third group adjoining to
said second column in said matrix are
coupled to a third bit line adjoining to said
second bit line in said plurality of bit lines.

Claims 70-72 differ from claims 67-69, respectively, in the replacement of "a parameter" with "an electrical value" and in the replacement of "settling a parameter" with "controlling an electrical value". As noted above in the support for claim 63, the "parameter" can be taken as the threshold voltage and the "settling" or "controlling" is the application of a programming pulse. Consequently, the support for claims 70-72 is respectively the same as that for 67-69 and will not be repeated to save space.

<ol> <li>An electrically non-volatile multi-</li> </ol>	The exemplary embodiments are all
level memory device comprising:	electrical non-volatile multi-level memory
	devices
a plurality of memory cells disposed	Figures 12 and 22 of the present
in matrix having rows and columns,	application and Figures 15a and 15b of '344.
wherein each of said plurality of	Figures 11c of '344 and 15A and 15B
memory cells has a threshold voltage	of the present application.
corresponding to data of two bits,	
wherein threshold voltages of said	Figures 11c of '344 and 15A and 15B
plurality of memory cells are allocated to one	of the present application.
of a first, a second, a third and a fourth	
threshold range,	
wherein said first threshold range	Figures 11c of '344 and 15A and 15B
indicates an erase state, and said second, said	of the present application.
third, said fourth threshold range indicate	
program states different from said erase state,	
wherein said second, said third and	Figures 11c of '344 and 15A and 15B

said fourth threshold range indicate mutually	of the present application.
different programming states,	
wherein a threshold voltage of a	Figures 11c of '344 and 15A and 15B
memory cell selected from said plurality of	of the present application.
memory cells is allocated in one of said first,	
said second and said third threshold range,	
and	
wherein control gates of memory cells	Figures 12 and 22 of the present
on the same row in said matrix are coupled to	application and Figures 15a and 15b of '344.
a word line of a plurality of word lines,	
a plurality of bit lines each of which	Figures 12 and 22 of the present
transfers information indicating data stored in	application and Figures 15a and 15b of '344.
a memory cell, wherein drain regions of	
memory cells on a first column in said matrix	
are coupled to a first bit line of said plurality	
of bit lines, drain regions of memory cells on	
a second column adjoining to said first	
column in said matrix are coupled to a second	
bit line adjoining to said first bit line in said	
plurality of bit lines and drain regions of	
memory cells on a third column adjoining to	
said second column in said matrix are	
coupled to a third bit line adjoining to said	
second bit line in said plurality of bit lines,	
a programming circuit programming	Figure 11e of '344: programming
ones of said plurality of memory cells to said	control, bit line and word line progr. pulse
programming states by using verify reference	See Figure 22 of the present application
parameters,	
a sense circuit which compares	Figure 11e, lower left portion, and
information indicating data stored in a	column 26, lines 51-65, of '344.

memory cell with a first reference parameter,	
a second reference parameter and a third	
reference parameter in parallel, in a normal	
read operation,	
wherein said first threshold range is	Figure 11c and column 26, lines 51-
lower than said second threshold range, said	65, of '344 and Figures 15A and 15B of the
second threshold range is lower than said	present application.
third threshold range, and said third threshold	
range is lower than said fourth threshold	
range,	
wherein said third reference parameter	Figure 11c and column 26, lines 51-
is higher than said second reference	65, of '344 and Figures 15A and 15B of the
parameter, and said second reference	present application.
parameter is higher than said first reference	
parameter,	
wherein said verify reference	Figure 11c and column 26, lines 51-
parameters have at least first and second	65, of '344 and Figures 15A and 15B of the
verify reference parameters,	present application.
wherein said first verify reference	Figure 11c and column 26, lines 51-
parameter is allocated between said second	65, of '344 and Figures 15A and 15B of the
threshold range and said third threshold	present application.
range, and said second verify reference	
parameter is allocated between said first	
threshold range and said second threshold	
range, and	
wherein said first verify reference	Figure 11c and column 26, lines 51-
parameter is settled between said second	65, of '344 and Figures 15A and 15B of the
reference parameter and said third reference	present application.
parameter, and said second verify reference	
parameter is settled between said first	

reference parameter and said second reference parameter.

 An electrically non-volatile multilevel memory device according to claim 73. wherein each of said plurality of memory cells has a floating gate, and a threshold voltage of a selected memory cell is allocated to one of said first, said second and said third threshold range from said fourth threshold range by being injected with hot electron to a floating gate of said selected memory cell.

For floating gate, see Figures 9-11 of the present application.

The threshold voltages are shown in Figures 15A and 15B of the present application.

Hot electron injection is specified in '344 at column 27, line 53, column 5, line 67, and column 10, line 62.

75. An electrically non-volatile multilevel memory device according to claim 74. further comprising,

a column select circuit which receives column addresses, and which couples selected hit lines to said sense circuite

1101, 1107, and 1109 of Figure 12, of the present application. Sense circuits1220 are shown in Figure 13.

level memory device according to claim 75. wherein each of said sense circuits has a first comparator which receives said information and said first reference parameter, a second column 26, lines 51-65, of '344, comparator which receives said information and said second reference parameter and a third comparator which receives said information and said third reference

Attorney Docket No.: SNDK. A06US5

76. An electrically non-volatile multi-

Figure 11e, lower left portion, and

pa		

77. An electrically non-volatile multilevel memory device according to claim 75, wherein each of said plurality of memory cells has a source region to which is supplied with a reference potential in said read operation.

80. For an electrically alterable non-

Figure 12 of the present application. Source region is denoted "S" and reference potential is "V<sub>S</sub>", where exemplary values are given in Tables 1 and 2 of Figures 26 and 27.

volatile multi-level semiconductor memory device including a plurality of non-volatile FET memory cells. multi-level memory cells, each of the multilevel memory cells including a floating gate FET having a channel with electrically alterable voltage threshold value, the plurality of non-volatile multi-level memory cells being disposed in a matrix of rows and columns, channels of multi-level memory cells of a group of the plurality of nonvolatile multi-level memory cells being coupled in parallel between a bit line and a reference potential, electrons being capable of being injected into the floating gate from the channel in each of the plurality of nonvolatile multi-level memory cells, a method of operating the electrically alterable nonvolatile multi-level semiconductor memory device, comprising:

All of the exemplary embodiments are multi-level non-volatile, floating gate FET memory cells.

Exemplary array structures with the described matrix structure are shown in Figures 15a and 15b of '344 and Figures 12 and 22 of the present application.

The injection mechanism is described briefly at column 1, lines 42-47, of '344 and in more detail for various cell embodiments beginning at column 5, line 33. See also page 11, lines 18-19 of Preliminary Amendment. non-volatile multi-level memory cell of the plurality of non-volatile multi-level memory cells to a state selected from a plurality of states including at least a first state, a second state, a third state and a fourth state in response to information to be stored in the one non-volatile multi-level memory cell,

setting a parameter of at least one

when one of the first third states is selected, verifying whether the parameter of the one non-volatile multi-level memory cell has been set to the one state, including comparing the parameter of the one nonvolatile multi-level memory cell with one of a plurality of verifying reference parameters including at least a first verifying reference parameter, a second verifying reference parameter and a third verifying reference parameter, the operation of setting the

by the operation of verifying that the parameter of the one non-volatile multi-level memory cell has been set to the one state.

multi-level memory cell. including comparing the parameter of the one nonvolatile multi-level memory cell, with a plurality of reading reference parameters including at least a first reading reference parameter, a second reading reference Amendment.

reading status of the one non-volatile

Setting is the program pulse, column 25, lines 16-20, of '344, and step 6 of Figure 23 of the present application. The states are shown in terms of threshold voltage in Figure 15A of the present application. See also Figure 11c of '344 for the current-voltage relation of the states, which is the same as Figure 15B of the present application.

See column 26, lines 18-35, of '344, Also, steps 4 and 5 of Figure 23 of the present application.

See also Figures 11c and 11e of '344 for the verifying reference parameters (the IREES) and the corresponding circuitry.

Column 25. lines 16-20 of '344 parameter being conducted until it is verified Also, the "repeating the operation..." corresponds to the loop of steps 4, 5, and 6 of Figure 23 of the present application.

> See again Figures 11c and 11e of '344 and the corresponding description beginning at line 34 of column 26 for the reading reference parameters (the Inss) and the corresponding circuitry. See also page 12, starting at line 6, of the Preliminary

parameter and a third reading reference	
parameter,	
wherein a conductivity value of the	Figures 11c of '344 and 15A and 15B
one non-volatile multi-level memory cell is	of the present application.
increased in order of the first state, the second	
state, the third state and the fourth state,	
wherein the first reading reference	Figures 11c and 11e and column 26,
parameter is allocated between the first state	lines 36-65, of '344.
and the second state, the second reading	
reference parameter is allocated between the	
second state and the third state, and the third	
reading reference parameter is allocated	
between the third state and the fourth state,	
wherein the first reading reference	See again Figures 11c and 11e of
parameter, the second reading reference	'344 and the corresponding description
parameter and the third reading reference	beginning at column 26, lines 36-65, of '344.
parameter are parameters for a normal read	
operation in which the information stored in	
the one non-volatile multi-level memory cell	
can be read out as output data of a plurality of	
bits,	
wherein the normal read operation	Figure 11e of '344 and column 26.
includes parallel-comparing the parameter of	lines 4-17. The sense circuits (SENSE
the one non-volatile multi-level memory cell	AMPs) are commonly connected in parallel
with the plurality of reading reference	to the BIT LINE and receive the respective
parameters using a plurality of sense circuits	reference currents.
including at least a first sense circuit, a	
second sense circuit and a third sense circuit,	
first input terminals of the first sense circuit,	
the second sense circuit and the third sense	

circuit are commonly supplied with the parameter of the one non-volatile multi-level memory cell, a second input terminal of the first sense circuit is supplied with the first reading reference parameter, a second input terminal of the second sense circuit is supplied with the second reading reference parameter and a second input terminal of the third sense circuit is supplied with the third reading reference parameter,

wherein the first verifying reference parameter is allocated above the first reading parameters and the reading reference reference parameter, the second verifying parameters is described in '344, column 26, reference parameter is allocated between the lines 51-65 first reading reference parameter and the second reading reference parameter and the third verifying reference parameter is allocated between the second reading reference parameter and the third reading reference parameter, and

The relation of the verifying reference

substantially a rectangle that has a first side, a second side, a third side and a fourth side, the first side and the second side intersect with

each other substantially perpendicularly, a plurality of word lines coupled with gate electrodes of floating gate FET's of the multilevel memory cells and the first side of the

wherein the plurality of non-volatile

multi-level memory cells of the matrix of the shown in Figures 15a and 15b of '344 and rows and the columns are disposed in Figures 12 and 22 of the present application.

The described matrix structure is

rectangle intersect with each substantially perpendicularly, a plurality of bit lines coupled with drains of floating gate FET's of the multi-level memory cells and the second side of the rectangle intersect with each other substantially perpendicularly, a row select circuit is disposed at the first side of the rectangle for coupling with the plurality of word lines, and peripheral circuitry, including a column select circuit, sense circuits, a data conversion circuit and latches, is disposed at the second side of the rectangle.

The method of operating the electrically alterable non-volatile multi-level memory according to claim 80.

wherein the operation of setting the parameter includes an crasure operation in application shows the erase operation as an which non-volatile multi-level memory cells of one of a byte, a block and a chip level can

Figure 23, step (1), of the present initial step in the programming.

The method of operating the electrically alterable non-volatile multi-level memory according to claim 81. wherein the operation of setting the

parameter includes a program operation in application. which electrons are injected into a floating gate of the one non-volatile multi-level

Figure 23, steps (4)-(6), of the present

be erased.

Claims 83-85 differ from claims 80-82, respectively, in the replacement of "a parameter" with "an electrical value" and in the replacement of "setting a parameter" with "controlling an electrical value". As noted above in the support for claim 80, the "parameter" can be taken as the threshold voltage and the "setting" or "controlling" is the application of a programming pulse. Consequently, the support for claims 83-85 is respectively the same as that for 80-82 and will not be repeated to save space.

Claims 86-88 are device claims that directly correspond, respectively, to method claims 80-82 on an element by element basis. Consequently, the support for claims 86-88 is again respectively the same as that for 80-82 and will also not be reneated to save space.

89. The electrically alterable nonvolatile multi-level memory according to claim 88.

wherein each of the plurality of bit lines transfers information indicating data stored in a memory cell, wherein drain Figures 12 and 22 of the present application. regions of said multi-level memory cells of said group in said matrix are coupled to a first bit line of said plurality of bit lines, drain regions of multi-level memory cells of a second group adjacent to said group in said matrix are coupled to a second bit line adjacent to said first bit line in said plurality of bit lines and drain regions of multi-level memory cells of a third group adjacent to said second group in said matrix are coupled to a third bit line adjacent to said second bit line in said plurality of bit lines.

The described matrix structure is shown in Figures 15a and 15b of '344 and Claims 90-93 differ from claims 86-89, respectively, in the replacement of "a parameter" with "an electrical value" and in the replacement of "setting a parameter" with "controlling an electrical value". As noted above in the support for claim 80, the "parameter" can be taken as the threshold voltage and the "settling" or "controlling" is the application of a programming pulse. Consequently, the support for claims 90-93 is respectively the same as that for 86-89 and will not be repeated to save space.

94. A non-volatile semiconductor	The exemplary embodiments are all
memory device comprising:	non-volatile semiconductor memory devices.
a plurality of non-volatile memory	Figures 12 and 22 of the present
cells each of which has a threshold voltage	application and Figures 15a and 15b of '344.
representing data of at least two bits, wherein	Figure 11c and column 26, lines 51-65, of
threshold voltages of the plurality of non-	'344 and Figures 15A and 15B of the present
volatile memory cells are shiftable among at	application.
least three threshold levels which indicate	
mutually different programming states and	
which also differ from a threshold level	
indicating an erase state;	
parameter generating circuitry	One embodiment uses the reference
generating a first programming reference	cells of Figure 17B of the present application.
parameter, a first read reference parameter, a	
second programming reference parameter, a	
second read reference parameter, a third	
programming reference parameter and a third	
read reference parameter; and	
sensing/program-verifying circuitry	1440 of Figure 17B of the present
receiving a parameter which represents	application; Figure 11e, lower left portion,
threshold voltage of one non-volatile memory	and column 26, lines 51-65, of '344.
cell, the first programming reference	
parameter, the first read reference parameter,	

EFS Filing Attorney Docket No.: SNDK.A06US5

the second programming reference parameter,	
the second read reference parameter, the third	
programming reference parameter and the	
third read reference parameter;	
wherein the first read reference	Figure 11c and column 26, lines 51-
parameter is allocated between a level	65, of '344 and Figures 15A and 15B of the
corresponding to the erase state and the first	present application.
programming reference parameter, the second	
read reference parameter is allocated between	
the first programming reference parameter	
and the second programming reference	
parameter, and the third read reference	
parameter is allocated between the second	
programming reference parameter and the	
third programming reference parameter,	
wherein the sensing/program-	Figure 17B of the present application;
verifying circuitry generates data of at least	Figure 11e, lower left portion, and column
two bits represented by the one non-volatile	26, lines 51-65, of '344. A program
memory cell threshold voltage, verifies	algorithm is shown in Figure 23 of the
whether the one non-volatile memory cell	present application.
threshold voltage is shifted to the threshold	
level indicating a selected one of the	
programming states, and programs the one	
non-volatile memory cell until it is verified	
that the one non-volatile memory cell	
threshold voltage has been shifted to that	
threshold level,	
wherein the first programming	Figure 11c and column 26, lines 51-
reference parameter is used for verifying	65, of '344 and Figures 15A and 15B of the
whether non-volatile memory cell threshold	present application.

voltages are shifted to a first threshold level of the three threshold levels, the first read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the first threshold level or to the threshold level indicating the erase state, and one of the first programming reference parameter and the first read reference parameter is shifted from and dependent upon the other.

'344. column 26, lines 60-65: "shifted by a fixed amount ..."

wherein the second programming reference parameter is used for verifying 65, of 344 and Figures 15A and 15B of the whether non-volatile memory cell threshold present application. voltages are shifted to a second threshold level of the three threshold levels, the second read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the second threshold level or to the first threshold level, and one of the second programming reference parameter and the second read reference parameter is shifted from and dependent upon the other, and

Figure 11c and column 26, lines 51-

wherein the third programming reference parameter is used for verifying 65, of 344 and Figures 15A and 15B of the whether non-volatile memory cell threshold present application. voltages are shifted to a third threshold level of the three threshold levels, the third read reference parameter is used for detecting

whether non-volatile memory cell threshold

by a fixed amount ..." Figure 11c and column 26, lines 51-

'344, column 26, lines 60-65: "shifted

voltages are near to the third threshold level or to the second threshold level, and one of the third programming reference parameter and the third read reference parameter is \$344, c shifted from and dependent upon the other.

'344, column 26, lines 60-65: "shifted by a fixed amount ..."

 A non-volatile semiconductor memory device according to claim 94.

wherein the parameter generating circuit which generates the first programming reference parameter, a second parameter the present application. generating circuit which generates the second parameter and the present application.

second read reference parameter, and a third parameter generating circuit which generates the third programming reference parameter The reference cells of Figure 17B of resent application.

and the third read reference parameter, and
wherein each of the first parameter
generating circuit, the second parameter
generating circuit and the third parameter
generating circuit includes an element
causing the corresponding one reference the present application.

The reference cells of Figure 17B of present application.

 A non-volatile semiconductor memory device according to claim 95, wherein each of the first parameter

parameter and the corresponding other reference parameter to have different values.

EFS Filing Attorney Docket No.: SNDK.A06US5 generating circuit, the second parameter generating circuit and the third parameter generating circuit further includes a reference cell which has substantially the same the present application. construction as each of said plurality of

memory cells, and the reference cell and the element of each parameter generating circuit cooperate to provide a predetermined difference between the corresponding read and programming reference parameters.

The reference cells of Figure 17B of

## A non-volatile semiconductor memory device according to claim 94.

wherein each read reference parameter is dependent upon the corresponding programming reference "shifted by a fixed amount ..." parameter.

'344, column 26, lines 60-65:

# A non-volatile semiconductor memory device according to claim 94,

wherein a conductivity value of the

one non-volatile memory cell is decreased in and 15B of the present application. order of the threshold level indicating the erase state, the first threshold level, the second threshold level and the third threshold level, and

Figure 11c of '344 and Figures 15A

volatile memory cells of one of a byte, a section, beginning on page 8, line 6, and block and a chip level can be shifted to the Figure 2 of the present application. threshold level indicating the erase state by

wherein threshold voltages of non-See the "Erase of Memory Structures"

an erase operation.	

A non-volatile semiconductor
memory device according to claim 98,
 wherein each of the plurality of non-

volatile memory cells has a floating gate to which electrons are capable of being injected from a channel.

Figures 9-11 of the present cation.

Aside from differing in the claim upon which they depend, claims 100, 102, 104, and 109 are the same as claim 98. Similarly, claims 101, 103, 105 and 110 are the same as claim 99, except for a change of dependence. Therefore, the support for claims 100, 102, 104, and 109 and claims 101, 103, 105 and 110 is the same as that given above for claim 98 and claim 99, respectively, and will not be repeated in order to same space.

# 106. A non-volatile semiconductor memory device according to claim 94, wherein the first, second and third read reference parameters are dependent

reference parameters, respectively.

third read reference parameters are dependent upon the first, second and third programming "shifted by a fixed amount ..."

memory device comprising:
a plurality of non-volatile memory
cells each of which has a floating gate and a
threshold voltage representing data of at least
two bits, wherein electrons are capable of
being injected into the floating gate, and
wherein threshold voltages of the plurality of

Attorney Docket No.: SNDK. A06US5

107 A non-volatile semiconductor

non-volatile semiconductor memory devices. Figures 12 and 22 of the present application and Figures 15a and 15b of '344. Figure 11c and column 26, lines 51-65, of '344 and Figures 15A and 15B of the present application.

The exemplary embodiments are all

non-volatile memory cells are shiftable	
among at least three threshold levels which	
indicate mutually different programming	
states and which also differ from a threshold	
level indicating an erase state; and	
sensing/program-verifying circuitry	1440 of Figure 17B of the present
receiving a parameter which represents the	application; Figure 11e, lower left portion,
threshold voltage of one non-volatile memory	and column 26, lines 51-65, of '344.
cell, a first programming reference parameter,	
a first read reference parameter, a second	
programming reference parameter, a second	
read reference parameter, a third	
programming reference parameter and a third	
read reference parameter;	
wherein the first read reference	Figure 11c and column 26, lines 51-
parameter is allocated to represent a level	65, of '344 and Figures 15A and 15B of the
between the threshold level indicating the	present application.
erase state and a level represented by the first	
programming reference parameter, the second	
read reference parameter is allocated between	
the first programming reference parameter	
and the second programming reference	
parameter, and the third read reference	
parameter is allocated between the second	
programming reference parameter and the	
third programming reference parameter,	
wherein the sensing/program-	Figure 17B of the present application;
verifying circuitry generates data of at least	Figure 11e, lower left portion, and column
two bits represented by the one non-volatile	26, lines 51-65, of '344. A program
memory cell threshold voltage, verifies	algorithm is shown in Figure 23 of the

whether the one non-volatile memory cell	present application.
threshold voltage is shifted to the threshold	
level indicating a selected one of the	
programming states, and programs the one	
non-volatile memory cell until it is verified	
that the one non-volatile memory cell	
threshold voltage has been shifted to that	
threshold level,	
wherein the first programming	Figure 11c and column 26, lines 51-
reference parameter is used for verifying	65, of '344 and Figures 15A and 15B of the
whether non-volatile memory cell threshold	present application.
voltages are shifted to a first threshold level	
of the three threshold levels, and the first read	
reference parameter is used for detecting	
whether non-volatile memory cell threshold	
voltages are near to the first threshold level or	
to the threshold level indicating the erase	
state,	
wherein the second programming	Figure 11c and column 26, lines 51-
reference parameter is used for verifying	65, of '344 and Figures 15A and 15B of the
whether non-volatile memory cell threshold	present application.
voltages are shifted to a second threshold	
level of the three threshold levels, and the	
second read reference parameter is used for	
detecting whether non-volatile memory cell	
threshold voltages are near to the second	
threshold level or to the first threshold level,	
wherein the third programming	Figure 11c and column 26, lines 51-
reference parameter is used for verifying	65, of '344 and Figures 15A and 15B of the
whether non-volatile memory cell threshold	present application.

voltages are shifted to a third threshold level of the three threshold levels, and the third read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the third threshold level or to the second threshold level wherein the first read reference See again Figures 11c and 11e of '344 parameter, the second read reference and the corresponding description beginning parameter and the third read reference at column 26, lines 36-65, of '344. parameter are parameters for a normal read operation in which the information stored in the one non-volatile memory cell can be read out as output data of a plurality of bits. wherein the normal read operation Figure 11e of '344 and column 26. includes parallel-comparing the parameter lines 4-17 and 39-42. The sense circuits representing the threshold voltage of the one (SENSE AMPs) are commonly connected in non-volatile memory cell with the plurality of parallel to the BIT LINE and receive the reading reference parameters using a plurality respective reference currents. of sense circuits including at least a first sense circuit, a second sense circuit and a third sense circuit, first input terminals of the first sense circuit, the second sense circuit and the third sense circuit are commonly supplied with the parameter from the one non-volatile multi-level memory cell, a second input terminal of the first sense circuit is supplied with the first read reference parameter, a second input terminal of the second sense circuit is supplied with the second read reference parameter and a second

input terminal of the third sense circuit is supplied with the third read reference parameter,

wherein the first read reference parameter is allocated to represent a level 65, of '344 and Figures 15A and 15B of the between the threshold level indicating the present application. erase state and the first threshold level the second read reference parameter is allocated to represent a level between the first threshold level and the second threshold level, and the third read reference parameter is allocated to represent a level between the second threshold level and the third threshold

Figure 11c and column 26, lines 51-

substantially at a midpoint between the first midpoint". threshold level and the second threshold level, and the level represented by the first read reference parameter is allocated toward the first threshold level from a midpoint between the threshold level indicating the crase state and the first threshold level.

wherein the level represented by the

On "midpoint", see '344, column 26. second read reference parameter is allocated line 63: "to place them closer to the

108. A non-volatile semiconductor memory device according to claim 107,

wherein an operation of shifting the one non-volatile memory cell threshold selected programming state includes a 23, steps (4)-(6) of the present application.

Figure 11e of '344 (bit line and word voltage to the threshold level indicating the line pulsing circuitry, waveforms) or Figure

level and

program operation in which electrons are
injected into the floating gate of the one non-
volatile memory cell by applying at least one
programming pulse to a bit line coupled to a
drain of the one non-volatile memory cell.

Claims 109 and 111 are, aside from a difference in dependence, the same as claim 98. Similarly, aside from a difference in dependence, claims 110 and 112 are the same as claim 99. Consequently, support for these claims is provided above and will not be repeated.

113. A non-volatile semiconductor	The exemplary embodiments are all
memory device comprising:	non-volatile semiconductor memory devices.
a plurality of non-volatile memory	Figures 12 and 22 of the present
cells each of which has a floating gate and a	application and Figures 15a and 15b of '344.
threshold voltage representing data of at least	Figure 11c and column 26, lines 51-65, of
two bits, wherein electrons are capable of	'344 and Figures 15A and 15B of the present
being injected into the floating gate, and	application.
wherein threshold voltages of the plurality of	
non-volatile memory cells are shiftable	
among at least three threshold levels which	
indicate mutually different programming	
states and which also differ from a threshold	
level indicating an erase state; and	
sensing/program-verifying circuitry	1440 of Figure 17B of the present
receiving a parameter which represents the	application; Figure 11e, lower left portion,
threshold voltage of one non-volatile memory	and column 26, lines 51-65, of '344.
cell, a first programming reference parameter,	
a first read reference parameter, a second	
programming reference parameter, a second	
read reference parameter, a third	

programming reference parameter and a third	
read reference parameter,	
wherein the first read reference	Figure 11c and column 26, lines 51-
parameter is allocated to represent a level	65, of '344 and Figures 15A and 15B of the
between the threshold level indicating the	present application.
erase state and a level represented by the first	
programming reference parameter, the second	
read reference parameter is allocated between	
the first programming reference parameter	
and the second programming reference	
parameter, and the third read reference	
parameter is allocated between the second	
programming reference parameter and the	
third programming reference parameter,	
wherein the sensing/program-	Figure 17B of the present application;
verifying circuitry generates data of at least	Figure 11e, lower left portion, and column
two bits represented by the one non-volatile	26, lines 51-65, of '344. A program
memory cell threshold voltage, verifies	algorithm is shown in Figure 23 of the
whether the one non-volatile memory cell	present application.
threshold voltage is shifted to the threshold	
level indicating a selected one of the	
programming states, and programs the one	
non-volatile memory cell until it is verified	
that the one non-volatile memory cell	
threshold voltage has been shifted to that	
threshold level,	
wherein the first programming	Figure 11c and column 26, lines 51-
reference parameter is used for verifying	65, of '344 and Figures 15A and 15B of the
whether non-volatile memory cell threshold	present application.
voltages are shifted to a first threshold level	

of the three threshold levels, and the first read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the first threshold level or to the threshold level indicating the erase state. wherein the second programming Figure 11c and column 26, lines 51reference parameter is used for verifying 65, of '344 and Figures 15A and 15B of the whether non-volatile memory cell threshold present application. voltages are shifted to a second threshold level of the three threshold levels, and the second read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the second threshold level or to the first threshold level wherein the third programming Figure 11c and column 26, lines 51reference parameter is used for verifying 65, of '344 and Figures 15A and 15B of the whether non-volatile memory cell threshold present application. voltages are shifted to a third threshold level of the three threshold levels, and the third read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the third threshold level or to the second threshold level. wherein the first read reference See again Figures 11c and 11e of '344 parameter, the second read reference and the corresponding description beginning parameter and the third read reference at column 26, lines 36-65, of '344, parameter are parameters for a normal read operation in which the information stored in the one non-volatile memory cell can be read

out as output data of a plurality of bits, wherein the normal read operation Figure 11e of '344 and column 26, includes parallel-comparing the parameter lines 4-17 and 39-42. The sense circuits representing the threshold voltage of the one (SENSE AMPs) are commonly connected in parallel to the BIT LINE and receive the non-volatile memory cell with the plurality of reading reference parameters using a plurality respective reference currents. of sense circuits including at least a first sense circuit a second sense circuit and a third sense circuit, first input terminals of the first sense circuit, the second sense circuit and the third sense circuit are commonly supplied with the parameter representing the threshold voltage of the one non-volatile memory cell, a second input terminal of the first sense circuit is supplied with the first read reference parameter, a second input terminal of the second sense circuit is supplied with the second read reference parameter and a second input terminal of the third sense circuit is supplied with the third read reference parameter, wherein the first read reference Figure 11c and column 26, lines 51parameter is allocated to represent a level 65, of '344 and Figures 15A and 15B of the between the threshold level indicating the present application. erase state and the first threshold level, the second read reference parameter is allocated to represent a level between the first threshold level and the second threshold level, and the third read reference parameter is allocated to represent a level between the

second threshold level and the third threshold level, and	
wherein the level represented by the second read reference parameter is allocated substantially at a midpoint between the first threshold level and the second threshold level, and the level represented by the third read reference parameter is allocated toward the second threshold level from a midpoint between the second threshold level and the	
third threshold level.	

Claims 115 and 117 are, aside from a difference in dependence, the same as claim 109. Similarly, aside from a difference in dependence, claims 116 and 118 are the same as claim 110 and claim 114 is the same as claim 108. Consequently, support for these claims is provided above and will not be repeated.

119. A non-volatile semiconductor	Claim 119 is the same as 113 except
memory device	for middle part of last element. See claim
	113 above for the omitted elements.
wherein the level represented by the	
second read reference parameter is allocated	
substantially at a midpoint between the first	On "midpoint", see '344, column 26,
threshold level and the second threshold	line 63: "to place them closer to the
level, and the level represented by the first	midpoint"
read reference parameter is allocated toward	
the first threshold level from a midpoint	
between the threshold level indicating the	
erase state and the first threshold level, and	
the level represented by the third read	

EFS Filing

reference parameter is allocated toward the
second threshold level from a midpoint
between the second threshold level and the
third threshold level.

Claims 121 and 123 are, aside from a difference in dependence, the same as claim 109. Similarly, aside from a difference in dependence, claims 122 and 124 are the same as claim 110 and claim 120 is the same as claim 108. Consequently, support for these claims is provided above and will not be repeated.

As presented above, it is respectfully submitted that the present application supports all of the currently pending claims and an early indication of their allowability is earnestly solicited. In the meantime, a phone call to the undersiened is invited should there be any ouestions.

Respectfully submitted.

Gerald P. Parsons

4/17/06 Date

Reg. No. 24,486

(415) 693-0194 (fax)

PARSONS HSUE & DE RUNTZ LLP 595 Market Street, Suite 19800 San Francisco, CA 94105 (415) 318-1160 (main) (415) 318-1163 (direct)